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TN00008

Power MOSFET frequently asked questions and answers

Rev. 2 — 31 October 2016

Technical note

Revision history

Rev	Date	Description
TN00008 v.2	20161031	a number of corrections made and new topics added
TN00008 v.1	20150806	initial version

Contact information

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Technical note

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1. Introduction

This technical note provides a number of important questions regarding the use of MOSFETs and the platforms required. Although it is focused on automotive applications, the principles can apply to industrial and consumer applications. It strives to provide clear answers to these questions and the reasoning behind the answers.

This document is intended for guidance only. Any specific questions from customers should be discussed with NXP power MOSFET application engineers.

2. Gate

2.1 Q: Logic Level Trench generation 3 types are specified with 15 V (V_{GS}). What is the technical reason for the reduction to 10 V for the Trench generation 6 logic level platform?

A: The Trench generation 3 platform is >10 years old. It was released to the best practice rules of the time. In particular, it was designed and assessed to meet the requirements of AEC-Q101. Production control and testing were established to ensure ongoing compliance to those requirements.

In the intervening years, the best practice rules have moved on. In particular, the understanding of gate oxide wear out has improved. It is now appreciated that meeting AEC-Q101 does not guarantee meeting modern reliability requirements. The market is looking for failure rates significantly lower than 1 ppm over the lifetime of >15 years.

In the Trench generation 6 data sheet, V_{GS} is rated at 175 °C and DC conditions. The gate can withstand 20 V at 25 °C for a short period (>1 hour on worst case parts). The capability is expected to be similar to competitor parts, often they state 20 V but do not specify the conditions for it.

Additional information

The Trench generation 6 platform specifies a gate voltage rating that exceeds the market reliability requirements and has production controls and tests to guarantee them.

The 10 V DC rating is conservative. Customer feedback is to set a clear, conservative but realistic limit on the data sheet. It ensures that engineers are guided to adopt good design practice and not use excessive overdrive.

For Trench generation 6 devices, use logic level parts where gate drive voltage is between 5 V and 10 V. Voltages of 15 V do not destroy any logic level part. Clearly, voltages between 10 V and 15 V are possible and have a corresponding range of lifetimes. However, the guidance is to use standard level parts where the gate voltage is >10 V for >100 hours in the life of the vehicle.

When new designs consider using a Trench generation 3 part, or earlier NXP technology, the same guidance should be used. It is because the gate oxide thicknesses are the same in Trench generation 3 and Trench generation 6. However, it should be appreciated that the same guarantees cannot be given because the tests and controls are not the same.

3. Thermal impedance (Z_{th}) curves

3.1 Q: When comparing Z_{th} curves in some data sheets, there appear to be some contradictions. From an R_{th} point of view, the BUK9Y38-100E (Trench generation 6) looks better (lower). However, from a Z_{th} (at less than 100 ms) point of view, the BUK9Y30-75B (Trench generation 3) looks better. The shape of the graphs indicates that a more advanced model or measurement was done on the Trench generation 6 part. Is this assumption correct?

A: The method for setting the Z_{th} curve has changed between the Trench generation 3 parts (2008) and Trench generation 6 (2012). The die size is also different which changes the Z_{th} and R_{th} characteristics.

Additional information

The earlier method used empirical models for Z_{th} (1 µs) and R_{th}, joined by an exponential line.

The latest method uses models for the Z_{th} generated by Computational Fluid Dynamics (CFD) simulation, verified by measurement.
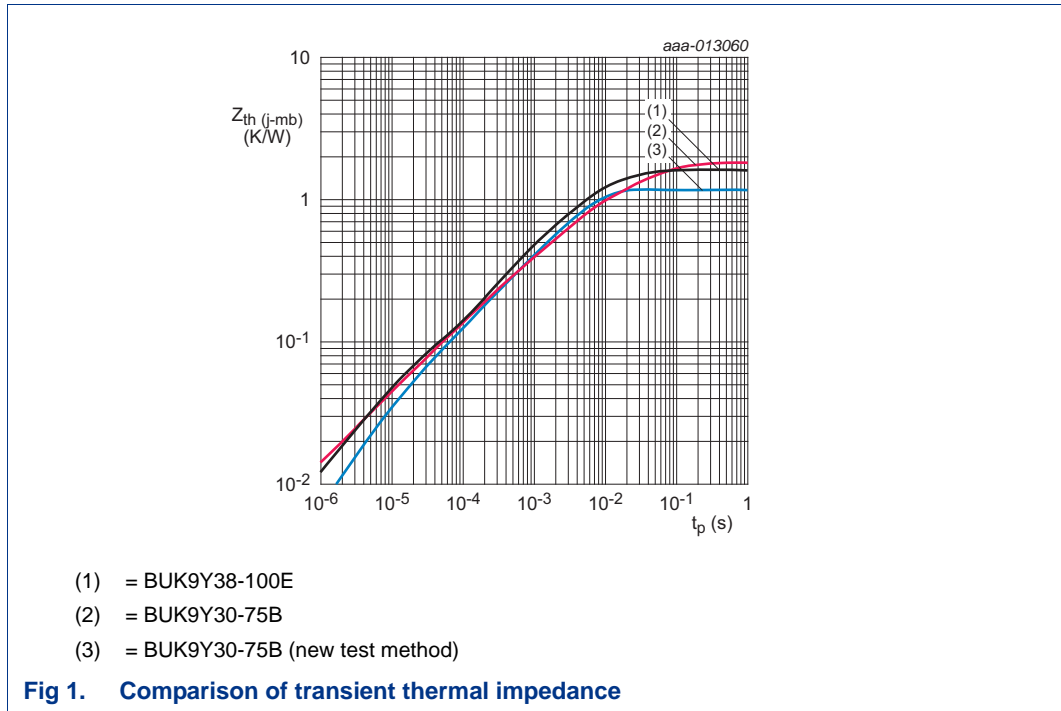
The dies in the 2 parts have different dimensions and therefore they have different Z_{th}.

The plots depicted in Figure 1 compare the data sheet curves for the single shot Z_{th}.

There is a good match between the limit lines for both parts. The biggest difference is in the region 1 ms to 20 ms.

The conclusion from this comparison, is that if the Trench generation 3 part is designed to work within these Z_{th} limits. The Trench generation 6 part is an excellent alternative that has a very high probability of working satisfactorily.

It is possible to assess how to rate the Trench generation 3 part using the new rules with a more accurate reflection of its true performance. Figure 1 shows the new line in comparison with the two data sheet lines.

(1) = BUK9Y38-100E

(2) = BUK9Y30-75B

(3) = BUK9Y30-75B (new test method)

Fig 1.   Comparison of transient thermal impedance

Although there is a difference in the R_{th}, it is probably unimportant. In practice, it is the $R_{th(j-amb)}$ that is the limiting factor for the design. The R_{th} of the Printed-Circuit Board (PCB) that is common to both parts, is dominant.

When considering the old test method with the new one for the BUK9Y30-75B, the other region of difference is below 10 μs. For pulse duration between 1 μs and 2 μs, the temperature rise (or $Z_{th(j-mb)}$) in the Trench generation 3 part, is only a half of what the original data sheet curve predicted. The importance of this factor depends on the application.

3.2 Q: It is understood that the values for thermal resistance listed in data sheets are based on controlled conditions that do not apply to typical applications. If this understanding is true, how is the proper thermal resistance/junction temperature accurately calculated?

A: This understanding is correct. To ensure reliability of the MOSFET, always limit the maximum junction temperature to 175 °C.

Additional information

It is understood that the typical values for thermal resistance listed in data sheets are based on controlled conditions that do not apply to typical applications.

Device characterization at a junction temperature of 25 °C is the accepted standard in the semiconductor industry. It is also most convenient for users to take measurements at this temperature.

How is the proper thermal resistance calculated?

Only a maximum value of thermal resistance is given on NXP MOSFET data sheets. The typical value is significantly less than the maximum. It is understood that thermal cycling can induce an increase in $R_{th(j-mb)}$ over the lifetime of the MOSFET.

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A tolerance margin is included in the data sheet maximum $R_{th(j-mb)}$ value which allows for an increase of over the lifetime of the MOSFET.

For worst case design analysis, always use the maximum value. Maximum $R_{th(j-mb)}$ given on the data sheet is evaluated from characterization measurements.

Its value is not dependent on temperature or other environmental conditions.

How is junction temperature calculated?

MOSFETs usually operate with a junction temperature greater than 25 °C due to temperature rise caused by the environment and/or power dissipation in the MOSFET.

If MOSFET power dissipation and mounting base temperature (T_{mb}) are known, MOSFET junction temperature can be calculated. Use Equation 1 to determine T_j.

$$T_j = P * R_{th(j-mb)} + T_{mb} \tag{1}$$

SPICE thermal models of MOSFETs provide an excellent means of estimating T_j by simulation. It is particularly useful when MOSFET power dissipation changes with time.

<u>Worked example for a BUK7Y12-40E:</u>

From the data sheet:

Maximum $R_{DS(on)}$ at 25 °C = 12 mΩ

Maximum $R_{DS(on)}$ at 175 °C = 23.6 mΩ

Maximum $R_{th(j-mb)}$ at 2.31 K/W

From the application data:

PWM frequency = 100 Hz

Maximum duty cycle = 50 %

V_{supply} = 14 V

R_{load} = 0.7 Ω

Maximum ambient temperature = 85 °C

Maximum PCB temperature = 100 °C

Calculation based on average power, ignoring any temperature fluctuation due to the power pulsing and also ignoring switching losses at 100 Hz:

Assume that the temperature of the MOSFET is initially 100 °C and its maximum $R_{DS(on)}$ is 18 mΩ. It is midway between 12 mΩ at 25 °C and 24 mΩ at 175 °C.

When conducting, the MOSFETs power dissipation $I^2R_{DS(on)}$ is:

20 × 20 × 0.018 = 7.2 W

The duty cycle is 50 %, so the average power dissipation = 7.2 × 0.5 = 3.6 W. It is assumed that the switching loss at 100 Hz can be ignored.

The rise of the MOSFET junction temperature, above the mounting base is:

2.31 × 3.6 = 8.3 K.

The maximum MOSFET die temperature in this situation is very safe at:

100 + 8.3 = 108.3 °C

To guarantee that the PCB temperature does not rise above 100 °C in an 85 °C ambient, the thermal resistance between PCB and ambient must be:

(100 − 85)/3.6 = 4.2 K/W

4. MOSFET body diode

4.1 Q: How much current can the MOSFET body diode carry?

A: The data sheet states the I_S capability for the diode. The power constraints are the same as for the MOSFET conduction. The diode is an integral part of the MOSFET structure. They are in effect the same size and have the same thermal properties. The MOSFET can carry the same current through the channel or in reverse through the body diode. The maximum steady state current in the diode is dependent on the total allowed power loss for the device. However, the diode current may be different from the channel current because the power dissipation may be different under the 2 modes of operation.

Additional information

The objective is to keep the junction temperature below $T_{j(max)}$ so it is necessary to calculate the diode dissipation. In a DC case, it is simply $I_F \times V_F$. It is equivalent to $V_{SD} \times I_S$ as used in the NXP MOSFET data sheet. For a worse case analysis, the max V_F of the data sheet should be used (normally 1.2 V).

Where the current is varying but in cyclic manner, the dissipation can be found using the equation:

$$\text{Power} = V_o \cdot I_{avg} + R_S \cdot I_{rms}^2 \tag{2}$$

where:

I_{avg} is the average diode current

I_{rms} is the RMS diode current

R_S is the slope of the I_{SD}/V_{SD} characteristic graph given in data.

V_o is typically where the R_S line meets the axis at I_{SD} = 0. For a conservative worst case analysis, use 1.2 V.

(1)   = characteristic at 25 °C

(2)   = idealized characteristic at 25 °C

(3)   = worst case idealized characteristic at 25 °C

Fig 2.   Diode characteristics
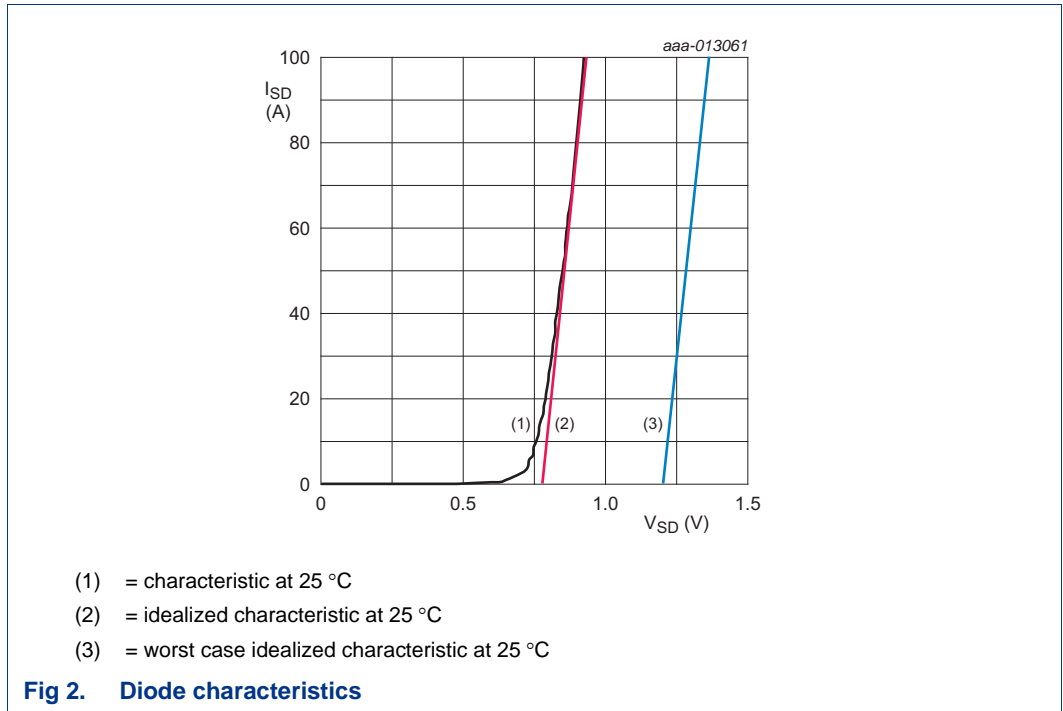
For transient currents, a simulation using the SPICE model of the diode is useful but care is needed because the model is for a typical part.

Once the dissipation is known, standard thermal analysis methods can be used to check that T_j is acceptable. It can include SPICE simulation using RC thermal models.

5. Safe operating area and linear mode operation

5.1 Q: The current derates with temperature. Is this limit based on power dissipation?

A: The most important factor in current derating or power derating is junction temperature. T_j is a function of power dissipation. Power dissipation is a function of I_D current and on-state resistance ($P = I_D^2 \times R$) when operating in the fully enhanced mode. It is the product of I_D and V_{DS} when operating between on and off states. The $R_{DS(on)}$ of a MOSFET, increases with increase in temperature. Therefore, for a given maximum power dissipation, the maximum current must be derated to match the maximum power dissipation. In NXP data sheets, graphs show the continuous drain current and normalized total power dissipation (see Figure 4) as a function of the mounting base temperature. These graphs can be used to determine the derating.

5.2 Q: Is it necessary to derate any limit (current, voltage, power etc.) to achieve high reliability?

A: If current, voltage, power, junction temperature, etc. are within NXP data sheet limitations, no additional derating is needed. In the data sheet, there is a power derating curve based on junction temperature. Junction temperature (T_j) is one of the most important factors for reliability. Particular care should be taken to extract enough heat from the device to maintain junction or die temperature, below rated values. The device should be operated within the SOA region. It should be derated if necessary (see Section 5.3) as recommended in the data sheet and it should be possible to obtain optimum reliability.

5.3 Q: How do I derate an SOA graph for temperatures other than 25 °C?

A: As an example, assume that the temperature required is 100 °C, instead of 25 °C. T_j rated is 175 °C for this automotive grade MOSFET. Derate the voltage when considering the effect of temperature on SOA performance (see Figure 3). To determine the new voltage (at temperature) for a fixed current, use the power derating line in Figure 4. For example, power at 100 °C = 50 % of power at 25 °C. Therefore, the 10 V line represents 5 V at 100 °C etc. It is explained in *Application Note AN11158*. If necessary, the SOA lines for 1 ms, 10 ms etc. can be extended at the same slope to the right.
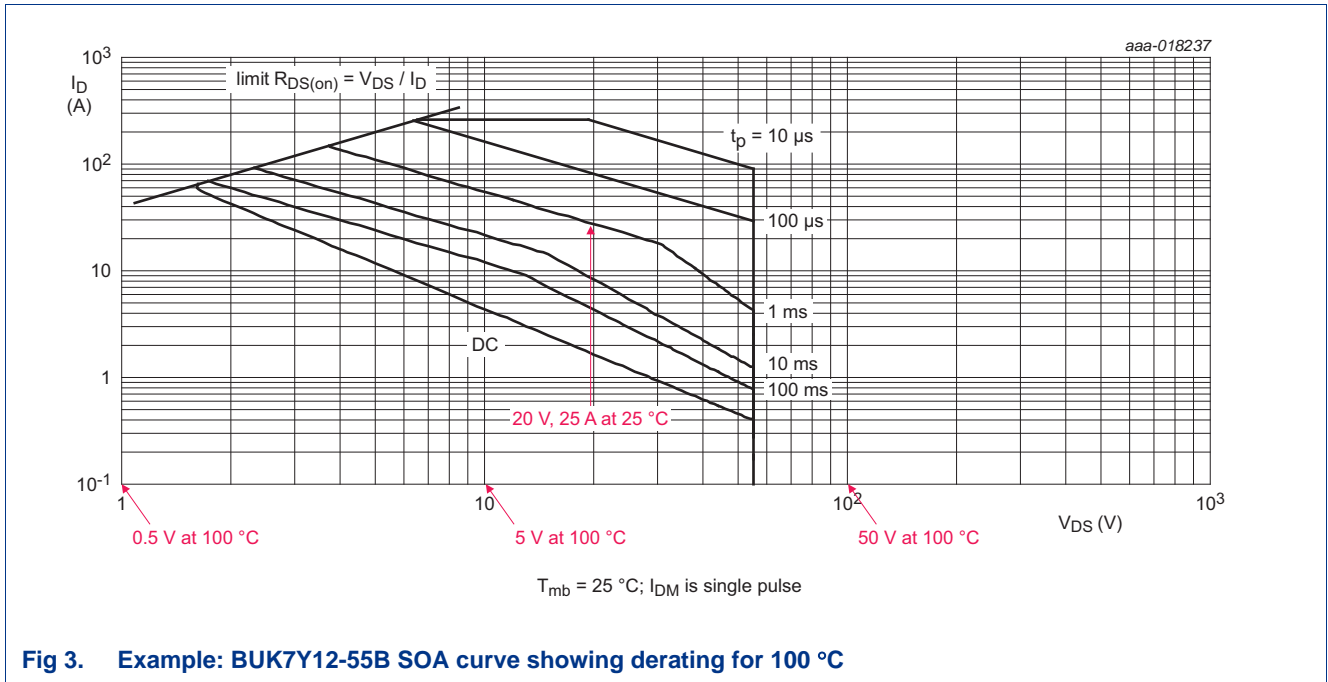
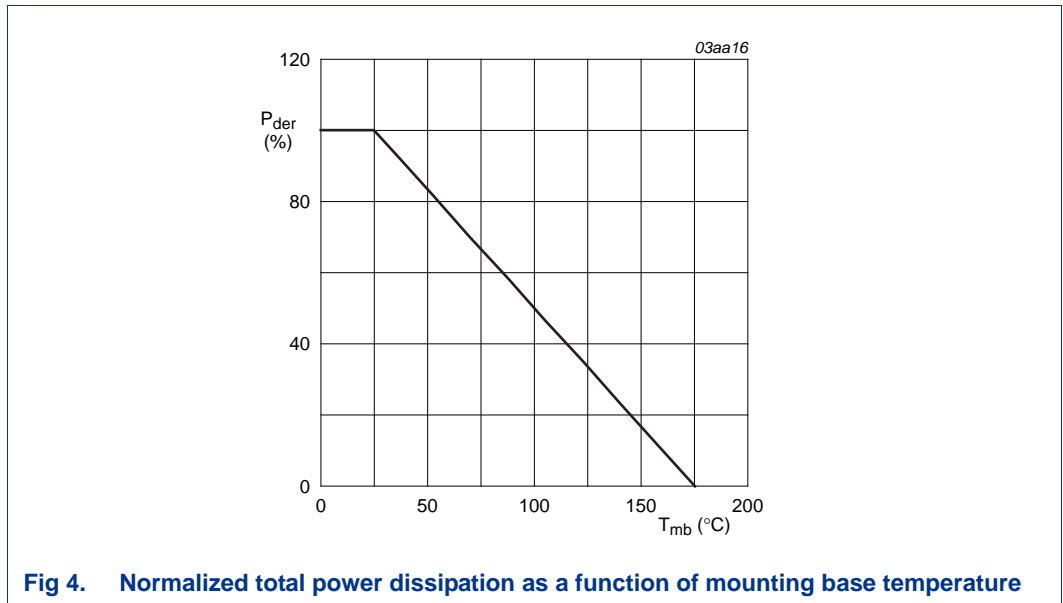**Fig 3.   Example: BUK7Y12-55B SOA curve showing derating for 100 ºC**

Fig 4.   Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100 \text{ \%}$$
(3)

5.4 Q: Is there a Spirito boundary limit line for linear mode operation?

A: The Spirito region or hot spotting issue with new higher density technologies may have more effect in the linear mode of operation. This effect is evident from the change in gradient in the limit lines for 1 ms, 10 ms and 100 ms at higher V_{DS} values (see Figure 3). The 1 ms, 10 ms, 100 ms and DC lines at higher V_{DS} values emphasize it. The reason is that most newer technologies pack more parallel fundamental cells to share more current

in a smaller die (lower $R_{DS(on)}$ per unit area). It leads to an increased thermal coupling between cells. Also, to attain higher current densities, the MOSFETs are designed with higher transconductance or gain ($g_{fs} = I_D/V_{GS}$). It enables them to carry higher currents even at lower V_{GS} values. However $V_{GS(th)}$ (threshold voltage) has a negative temperature coefficient which leads to a higher zero temperature coefficient crossover value. For various reasons, the distribution of temperature in the die is never perfectly uniform. Therefore, when the device is operated for extended periods in linear mode, hot spotting occurs. Due to the shift in threshold voltage, there is a risk of thermal runaway and device destruction where the hotspots form. Because of these reasons, special care should be taken when using trench or planar MOSFETs for linear applications. Ensure that operation remains within the data sheet SOA limits.

5.5 Q: Regarding the SOA curve for the 1 ms and 10 ms curves, there is a bend-down at higher voltages and low currents. Why does this bending disappear for longer and shorter pulse times?
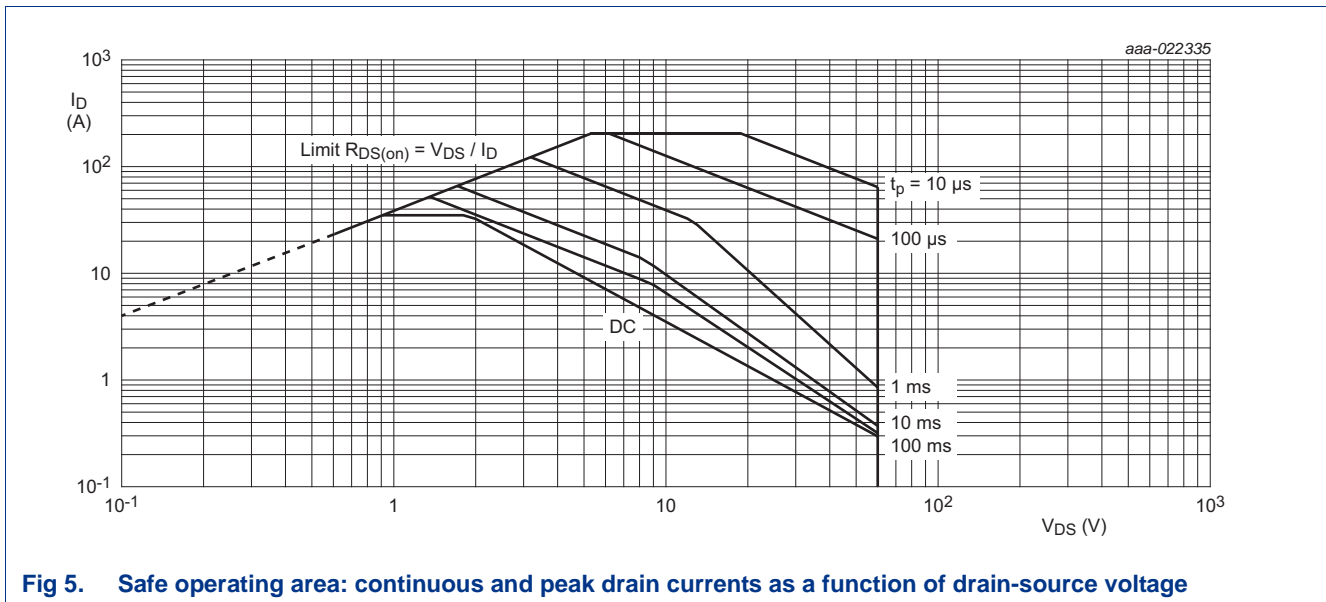
Fig 5. Safe operating area: continuous and peak drain currents as a function of drain-source voltage

A: The inflexion points on the 1 ms and 10 ms lines represent the points where the 'Spirito' effect starts. At higher I_D, the lines represent constant power (P); at lower I_D, P decreases as I_D decreases. The 100 ms and DC lines are straight, but have higher negative gradients than constant power lines, i.e. power also decreases as I_D decreases. The flat portion of the DC line represents package maximum I_D.

The Spirito effect is a form of electro-thermal instability i.e. uneven die heating leading to hot-spot formation. It happens because $V_{GS(th)}$ has a Negative Temperature Coefficient (NTC) at I_D values below I_{ZTC} (zero temperature coefficient current). The consequence is to reduce MOSFET power dissipation capability in lower I_D zones of the SOA chart.

Measurement at DC, 100 ms, 10 ms and 1 ms establishes SOA capability. The 100 μs and 10 μs lines on this graph are theoretical constant power lines. They are realistic, as the Spirito effect is much less significant at higher currents and shorter pulse periods.

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Reliable 100 μs SOA measurement capability has recently been achieved, so future data sheets include 100 μs SOA lines based on measured data. It is now evident that the Spirito effect is apparent at 100 μs. Consequently, from 2016, new MOSFET releases have a measured 100 μs SOA line in their data sheet SOA graph.

See *AN11158* for further information.

5.6 Q: How does NXP ensure compliance with the SOA curve during series production?

A: The factors influencing the compliance of the MOSFET with the data sheet SOA graph are:

- the uniformity of the MOSFET cells across the active (trench) surface of the die
- the integrity and uniformity of the die attachment (the solder layer between the die bottom (drain) surface and mounting base)

Cell uniformity must be good for the MOSFET to work. However, cell uniformity can never be perfect and there is always some variation between cells.

The integrity of the soldering to attach the die must be good without voids or die tilt. If not, the local (junction to mounting base) thermal impedance varies with location across the die. It gives uneven cooling. Uneven die surface cooling may be due to either or both of the factors stated. However, the consequence is the same i.e. SOA non-compliance with the data sheet graph.

In production, linear mode power pulse tests are used to stress the MOSFET thermally. If the die cooling is not sufficiently uniform, hotspots can form and the device parameters can change more than expected. A decision to reject parts can be made based on the results.

5.7 Q: How can a part be identified when it is designed for linear mode operation?

A: While all NXP MOSFETs can be used in linear mode operation, some NXP MOSFETs are designed specifically to be used in linear mode. The device description in the data sheet states that the device is suitable for operation in linear mode. To determine the suitability for operation in linear mode, perform a thorough analysis of the SOA graph. This analysis includes derating the SOA graph for junction temperatures above 25° C. The naming convention indicates that the MOSFET is designed for linear mode applications.

5.8 Q: For parts designed for linear mode operation, are there any restrictions (such as the Spirito boundary)?

A: Even if a MOSFET is intended for use in linear mode applications, the part must not be operated outside its SOA. Post 2010, all NXP MOSFETs have a measured SOA characteristic. The limit of linear mode capability on NXP parts is shown in the SOA characteristic. As a result, the boundary of what is safe is established via measurement rather than calculation. The Spirito capability limit is shown in the SOA characteristic.

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6. Avalanche ruggedness and Unclamped Inductive Switching (UIS)

6.1 Q: Are trench designs susceptible to the UIS issue (parasitic BJT turn-on)?

A: In general - Yes, but NXP Trench MOSFETs are designed to suppress this effect. The trench structure, unlike planar, can be very easily designed to suppress parasitic turn on of the BJT. For new NXP MOSFET technologies, the failure mechanism is thermal, which represents the limit of achievable UIS performance. Planar (on the left in the diagram) and trench (on the right in the diagram) MOSFET technologies, are shown in Figure 6. In the trench case, a design feature in the source contact effectively short circuits the base-emitter of the parasitic BJT. In older planar technology, the shorting of base to emitter of the parasitic bipolar is not as effective. It is due to the longer path length in the n and p regions.
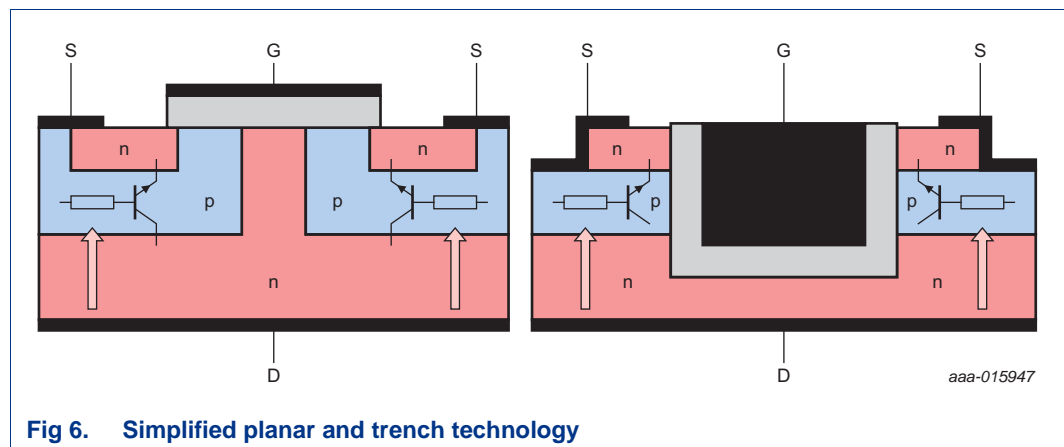
Fig 6. Simplified planar and trench technology

6.2 Q: Why are planar designs susceptible to failure during UIS?

A: All MOSFETs are susceptible to failure during UIS. It depends on whether the MOSFET T_j reaches the intrinsic temperature of silicon. Furthermore, if the parasitic BJT is triggered, they can fail even earlier. It is because the BJT can be switched on relatively quickly but is slow to switch off. Current can then crowd in a certain part of the device and failure results. Newer NXP trench technologies are less vulnerable to triggering of the BJT than planar designs. See Section 7.1 and the additional information associated with Section 6.3.

6.3 Q: How are parts constructed to minimize failure during UIS?

A: The base emitter path in the silicon design is designed to minimize the risk of triggering the parasitic BJT.

Additional information

There are two strategies employed to prevent triggering of the parasitic BJT:

1. Reduce the avalanche current per cell - To reduce the avalanche current per cell, there must be a higher cell density. It is easily achieved with trench technologies but more difficult with planar devices. If improvements in planar technologies are seen, it is likely that modern fabrication equipment achieves a high enough cell density. Increasing cell density too much, deteriorates linear mode performance (Spirito

boundary occurs sooner), so cell density is a trade-off. For this reason, NXP has not been as aggressive as other trench MOSFET manufacturers in achieving very high cell densities. The target is to ensure that the thermal limit in UIS is achieved.

2. Ensure that the current flow during avalanche does not flow through the base-emitter region of the BJT. This feature is the significant advantage of trench over planar. The parasitic bipolar is formed between the source of the MOSFET, the body region (i.e. channel) and the epi region (i.e. the drain). If there is enough avalanche current through body junction, there may be enough voltage developed to bias on the BJT leading to device destruction. In NXP devices, a modified source contact is used. This contact collects any avalanche current, preventing it from biasing the BJT on.

For planar devices, strategies include reducing the gain of the BJT by placing high doped implants close to the channel. It is similar to (2) in intention but it is not as effective.

6.4 Q: Is 100 % UIS testing required on MOSFETs?

A: UIS testing is a fundamental part of NXPs defect screening procedures. It is applied to all devices. The test is designed to increase the junction temperature to $T_{j(max)}$.

6.5 Q: I have parts not capable of parasitic BJT turn-on. Why?

A: Devices fail at the thermal limit. At the thermal limit, the silicon becomes intrinsic and blocking-junctions cease to exist. It is considered to be the only UIS-related failure mechanism in our devices.

6.6 Q: What is the chart accuracy for avalanche current versus time in avalanche, or energy versus junction temperature?

A: Avalanche current versus time graphs are based on conditions that take a device to $T_{j(max)}$ and therefore, our ruggedness screening covers them. All NXP MOSFETs are ruggedness tested during assembly and characterized during development. The graphs are accurate and provide the worst case capability of the device to ensure reliability.

6.7 Q: For energy versus junction temperature charts (if applicable), how is the inductance, maximum current, time in avalanche etc., determined from the chart?

A: A temperature rise model is used, which is shown in *AN10273 Power MOSFET single-shot and repetitive avalanche ruggedness rating*.

Additional information

Although energy levels for UIS are often quoted on data sheets, a single number can be misleading. Therefore a graph is provided, that outlines conditions that take junction temperature to $T_{j(max)}$. The user must determine the current/time in avalanche based on the particular conditions. Examples are provided in *AN10273 Power MOSFET single-shot and repetitive avalanche ruggedness rating*.

6.8 Q: Are repetitive avalanche ratings the same as for a single pulse?

A: No. The repetitive avalanche ratings are lower than the single pulse rating. Refer to the product data sheet for the device capability. An example is shown in Figure 7.

Repetitive means that the avalanche event is an intended operating condition for the device.

Similarly, single-shot means that the MOSFET is expected to experience an avalanche event as a result of some unintended fault condition. Only 1 fault can occur at a time, the MOSFET must cool to the starting temperature and the junction temperature must not exceed 175 °C. Degradation of device characteristics is likely after a relatively low number of occurrences.

NXP shows both single shot and repetitive avalanche capability in the MOSFET data sheet. Generally, the repetitive current is 10 % of the single shot current capability for a given inductor (so the time in avalanche is shorter, see Figure 7 and Section 6.14).

For calculating repetitive avalanche ratings, calculate the starting junction temperature for each avalanche incident independently. The calculations are based on the frequency and duty cycle of avalanche condition and summed over the entire period of expected repeated avalanche. This topic is discussed in detail in NXP Application Note *AN10273 Power MOSFET single-shot and repetitive avalanche ruggedness rating*.

6.9 Q: Are there any special failure modes associated with repetitive avalanche?

A: The device can sustain small amounts of damage with each avalanche event and over time they can accumulate to cause significant parametric shifts or device failure. NXP has performed research into this area and provides the repetitive ratings in the data sheet. See also NXP Application Note *AN10273 Power MOSFET single-shot and repetitive avalanche ruggedness rating*.

6.10 Q: How does the increase in cell density affect avalanche capability of MOSFETs?

A: There are two failure modes: current (parasitic BJT turn-on) and thermal. Cell density has implications for these failure modes.

Current - If enough avalanche current flows through a cell, a voltage drop occurs in the p-region of the device as the avalanche current flows to the source contact. This volt drop occurs in the base of a parasitic bipolar device. In this mode, the resistance in the p-region/base and the avalanche current ($I = V/R$) are important. Once V_{BE} reaches the bipolar switch-on threshold, the MOSFET is destroyed (V_{BE} reduces with temperature). So at higher cell densities, for the same avalanche current, there are more cells and current per cell is reduced. Each individual cell has less current and is less likely to trigger the parasitic device. It means that the total die current, required to cause a device to fail, increases. Additionally, since the cell is smaller, the path through the p-region to the source contact is reduced. It makes it even harder to trigger the parasitic device and again increases the current required to destroy the device.

Thermal - If the avalanche current is such that the parasitic BJT is not triggered, the device heats up. If the avalanche energy is sufficient, the silicon die reaches temperatures at which the device starts to become intrinsic. The blocking-junction no longer exists, resulting in the destruction of the device. It is what is meant when a

reference is made regarding failure due to reaching the thermal limit of a device. If the failure mode is thermal, changes in technology cannot improve things significantly. New technologies are generally more robust in avalanche conditions. Note, if a thermal limit is reached, the only solution is to improve the thermal impedance at the device level. Moving to a smaller die can be detrimental.

Summary - New technologies improve the high current avalanche capability of a device due to increased cell density and reduced parasitic NPN base resistance. Lower current, higher energy (i.e. longer duration) avalanche capability is unchanged.

6.11 Q: How many times can a device sustain single avalanche events?

Example - A device has an avalanche event once in two months so how many cycles of such an avalanche frequency can the device sustain? This question relates more to quality and reliability but it is important nonetheless.

A: Refer to Section 6.8 of this document. For the answer to this question, refer to *Section 2.4.3 of AN11158* and all of *AN10273*.

Additional information

Keep each avalanche event within the safe limits for repetitive operation specified on the data sheet and T_j below 175 °C. There should be no degradation of the MOSFET characteristics and no impact on MOSFET quality or reliability. There are some applications where MOSFETs are repetitively avalanched (e.g. some engine controllers) and the reliability is good. Although this condition takes V_{DS} beyond the data sheet maximum, the data sheet also specifies a maximum avalanche energy.

Extensive avalanche testing is performed on NXP MOSFETs. All the indications are that they are very robust. It is understood that most MOSFETs in automotive applications are likely to experience avalanche conditions at some stage during their lifetime. It could be due to occasional fault conditions or as a consequence of the circuit design (e.g. ABS solenoid valve driver MOSFETs).

6.12 Q: Is it possible for the avalanche current on a device to exceed the package maximum current but not the die maximum current?

A: The current specified in the avalanche graph should not be exceeded. It is restricted to the DC rated current. The device factory test defines the limit which is guaranteed for the device.

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6.13 Q: How is the avalanche rating on the body diode obtained (testing or modeling)? If it is tested, how is it tested and what circuit model is used?

A: The avalanche rating is modeled first and the results are then verified by testing to destruction. The test circuit used is similar to the one defined in *JESD24-5*. For spice modeling, the reverse diode characteristics can be defined and modeled. By adding an RC thermal model of the Z_{th} characteristic, it is possible to estimate the T_j of the device.

<u>Additional information</u>

The body diode of the MOSFET is not a single circuit element, but a structure distributed throughout the MOSFET. There is a diode element associated with each cell. In behavior terms, it can be represented as a single (Zener) diode in parallel with the single MOSFET (representing the sum of all the cells). The design of the MOSFET determines the avalanche rating. Its representation in the model is based on parameters measured during characterization testing.

The constraints are the same as for the MOSFET conduction. Diodes are an integral part of the MOSFET structure. They are in effect the same size and have the same thermal properties. The objective is to keep the junction temperature below $T_{j(max)}$ so it is necessary to calculate the diode dissipation.

For transient currents, the simulation using the spice model of the diode is useful but care is needed because the model is for a typical part.

Once the dissipation is known, standard thermal analysis methods can be used to ensure that T_j is acceptable.

6.14 Q: How is the repetitive avalanche safe operating area derived in the data sheet graph? The repetitive avalanche SOA curve seems to be the same as single-shot T_j = 170 °C.

A: The repetitive line is the line for a start temperature of 170 °C. It is because it predicts a temperature rise of 5 °C which is the maximum permissible rise from any starting temperature (see *AN10273*). It also corresponds to 10 % of the single-shot current using the same inductor value, see <u>Figure 7</u>.

<u>Additional information</u>

The reason it applies to any temperature is because the temperature does not strongly influence the wear-out caused by repetitive avalanche. The strongest influence is the current.

The avalanche current is composed of high energy charge carriers moving through the depletion region. As they pass through, they can collide with the Si structure. There is a chance that a high energy carrier (sometimes called a hot carrier) is produced that collides with the gate oxide causing damage. It is not completely destroyed but it does cause it to wear out, which is observed as parameter variation.

Higher currents mean more electrons, more collisions and more frequent damaging events leading to faster wear-out and lower reliability. The target should be a failure level <0.1 ppm over the full vehicle life. Experiments indicate that if repetitive current is limited to 10 % of single-shot current capability for $T_{j(start)}$ = 25 °C, it results in a T_j increase of 5 °C. There is no significant degradation of the device.

For example: A 15 mH inductor carrying ~19 A gives an avalanche time of ~5 ms. It has a peak temperature rise of 150 °C putting it on the limit line for $T_{j(start)}$ = 25 °C.

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By reducing the current to 10 % = 1.9 A, t_{AL} reduces to ~500 µs and the temperature rise is 5 °C.

(1) = characteristic at 25 °C

(2) = characteristic at 150 °C

(3) = repetitive characteristic at <170 °C

(4) = inductor characteristic

Fig 7.   Avalanche safe operating area
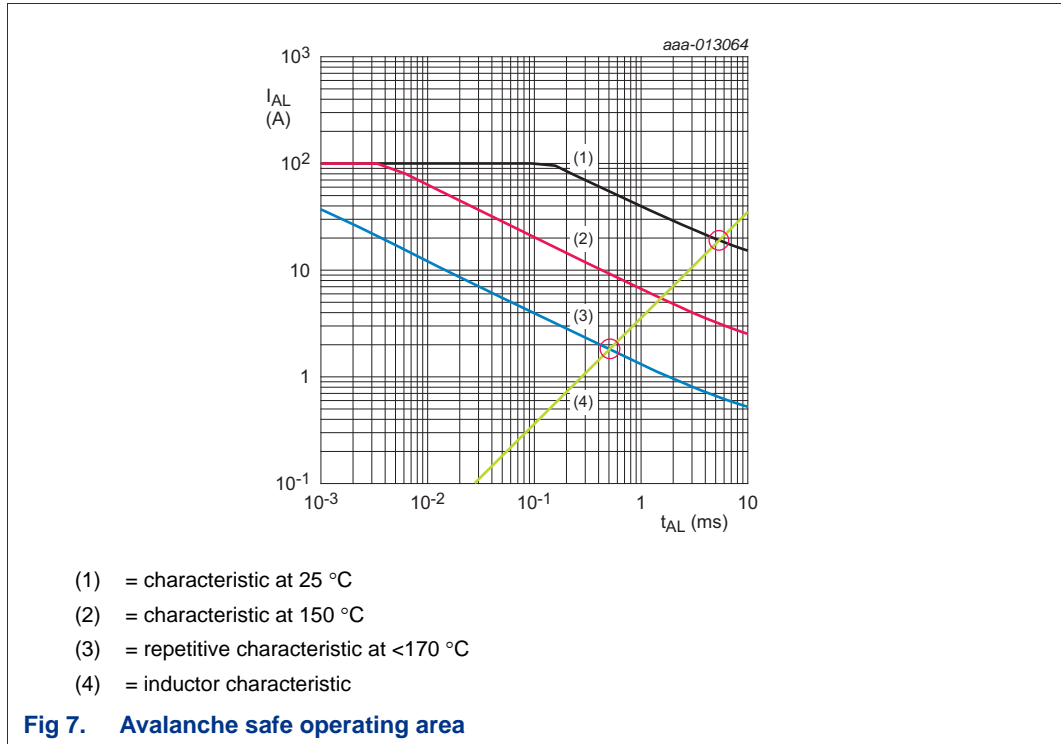
7. Capacitive dV/dt issues

7.1 Q: Is there a particular capacitance or charge ratio that should be used to prevent turn-on, or is it circuit dependent?

A: The capacitive dV/dt turn-on is strongly circuit dependent.

Additional information

If the dV/dt across the MOSFETs drain to source is too high, it may charge C_{GD}, which is the capacitance between drain and gate, inducing a voltage at the gate. The gate voltage depends on the pull down resistor of the driver based on Equation 4:

$$V_{GS} \ = \ R_{driver}{}^{*}C_{GD}{}^{*}dV/\mathrm{dt} \tag{4}$$

In some bipolar drive circuits, such as emitter follower derived circuits, the problem is increased. It is because the driver cannot pull the gate down to 0 V and has approximately 0.7 V offset.

It is also important that the driver is referenced to the MOSFET source and not to signal ground, which can be significantly different in voltage.

The ratio of C_{GD} to C_{GS} is a factor but a good drive circuit is the critical factor.

Even if a V_{GS} spike is present, it is safe for the MOSFET as long as the dissipation is within thermal limits and MOSFET SOA limits.

7.2 Q: How are parts constructed to minimize this effect?

A: NXP MOSFETs are designed with a high threshold at high temperatures and we check V_{GS} threshold at 25 °C is within data sheet limits. Logic level devices are designed and guaranteed to have a minimum threshold voltage >0.5 V even at 175 °C.

Additional information

Maintain a reasonable ratio between C_{GD} and C_{GS}. The gate network structure of the device is designed to have good control of all areas of the die.

7.3 Q: How is dV/dt characterized?

A: It is usually measured in a half-bridge test circuit. It is a measure of the device dV/dt during body diode reverse recovery. This data is not normally published in the data sheet. This dV/dt is in practice the highest dV/dt the device experiences.

Additional information

Failure due to dV/dt is not something seen in modern low-voltage MOSFETs however, dV/dt is normally characterized for NXP MOSFETs. The failure mode is that the capacitive current resulting from dV/dt, triggers the parasitic BJT. However, as the voltages are low (dV/dt is more an issue > 600 V) a current/charge high enough to trigger the parasitic BJT cannot be generated.

7.4   Q: What diode or other parameters are important to assess susceptibility? For example, maximum dV/dt and maximum I_F.

A: High dV/dt can induce glitches onto the gate of the MOSFET. A snubber can help to reduce dV/dt and the magnitude of the V_{DS} spike if significant. The ratio of C_{oss} at low V_{DS} compared to C_{oss} value at high V_{DS} is an indicator of the non-linearity of C_{oss}. A very high ratio can indicate that the device can generate a high dV/dt. Gate driver circuit design can reduce the gate glitch, see Section 7.1. The ratio of Q_{GD} to Q_{GS} and the gate threshold voltage can be used to indicate the susceptibility of the device to gate glitches.

7.5   Q: Is trench technology sensitive to this phenomenon?

A: In theory, all MOSFETs are.

Additional information

dV/dt induced turn-on of the parasitic bipolar transistor is not known as an issue in low voltage NXP MOSFETs. If UIS parasitic turn-on is solved, then dV/dt induced turn-on is also solved. Refer to Section 6.1 and Section 6.3 for more information.

7.6   Q: Does a soft recovery body diode give lower dV/dt and if so, how is it designed and fabricated into the part?

A: Soft recovery does reduce the dV/dt. Although dV/dt is not an issue for the MOSFET, a lower dV/dt is better for EMI, voltage spikes and crosstalk. The design and manufacture is very specialized, involving proprietary information.

7.7   Q: How does temperature influence this sensitivity to dV/dt and why?

A: At high temperatures, it is easier to trigger a parasitic bipolar as its V_{BE} reduces. But if the BJT is effectively shorted out and current diverted away from it, as discussed in Section 6.1, then it is not an issue.

7.8   Q: Can NXP provide R_B, C_{DB}, V_{BE} saturation values in the parasitic BJT model, as shown in Figure 8?

A: These values are required to be able to calculate Equation 6. The aim is to obtain a dV/dt value to check if parasitic BJT turns on, leading to device failure. It is impossible to measure the characteristics of the parasitic bipolar transistor as its terminals cannot be accessed independently of the MOSFET terminals. A parasitic bipolar transistor is always created when a MOSFET is fabricated. Referring to Figure 8, it can be seen that there are two current paths which could cause MOSFET problems. Current I_1 flows via C_{GD} and depending on C_{GS} and R_G it can cause the MOSFET to switch on momentarily. It is often referred to as a gate glitch. Current I_2 flows via C_{DB} and R_B which can potentially switch on the parasitic BJT

Additional information

$$V_{GS} \ = \ I_1 {}^* R_G = R_G {}^* C_{GD} {}^* dV/dt \tag{5}$$

$$V_{BE} \ = \ I_2 {}^* R_B = R_B {}^* C_{DB} {}^* dV/dt \tag{6}$$
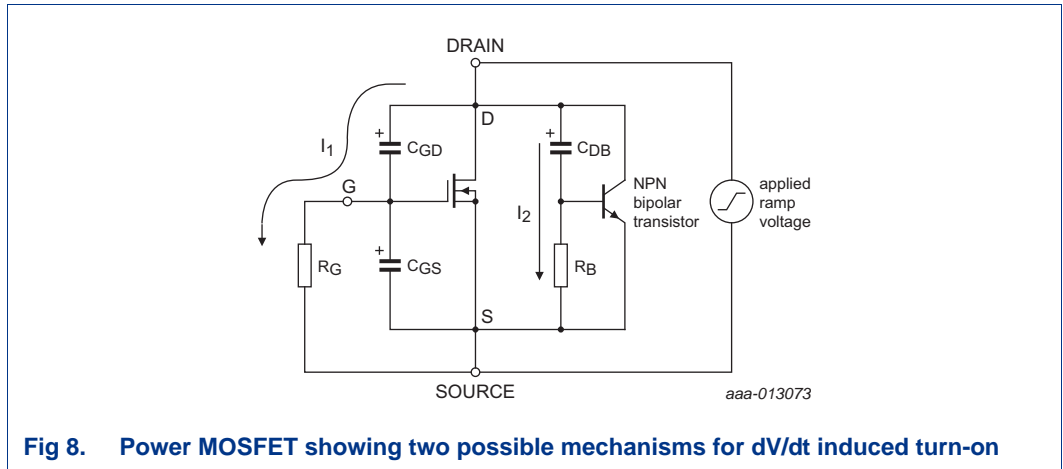
Fig 8. **Power MOSFET showing two possible mechanisms for dV/dt induced turn-on**
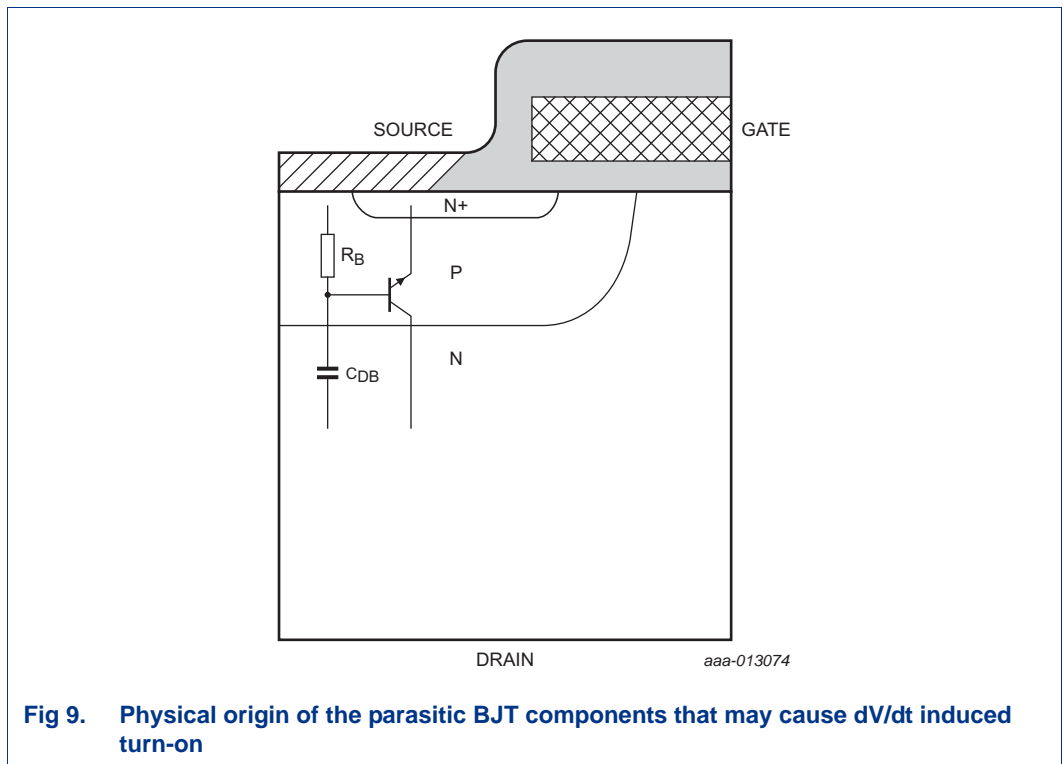
Fig 9. **Physical origin of the parasitic BJT components that may cause dV/dt induced turn-on**

Additional information

Early lateral MOSFETs (structure shown in Figure 9), were susceptible to failure caused by the turn-on of this parasitic transistor.

However, trench MOSFETs, as manufactured by NXP, are much more immune to this failure mechanism.

The gate structure is located in trenches in the die surface rather than it being a horizontal layer on the die surface. This structure means that the short-circuiting of the base emitter junction of the parasitic bipolar transistor (to prevent its turn on), is much more effective.

As the generations of trench MOSFETs have progressed, feature dimensions (trench pitch) have reduced, making the parasitic bipolar transistor even more immune to being turned on.

Figure 10 shows the structure of a trench generation 6 device. The parasitic bipolar inhibition is particularly good in this structure due to the very short base to emitter length. The source metal short-circuits the p-n junction near the source contact, making it difficult to get a V_{BE} high enough to turn on the parasitic BJT.

aaa-013075
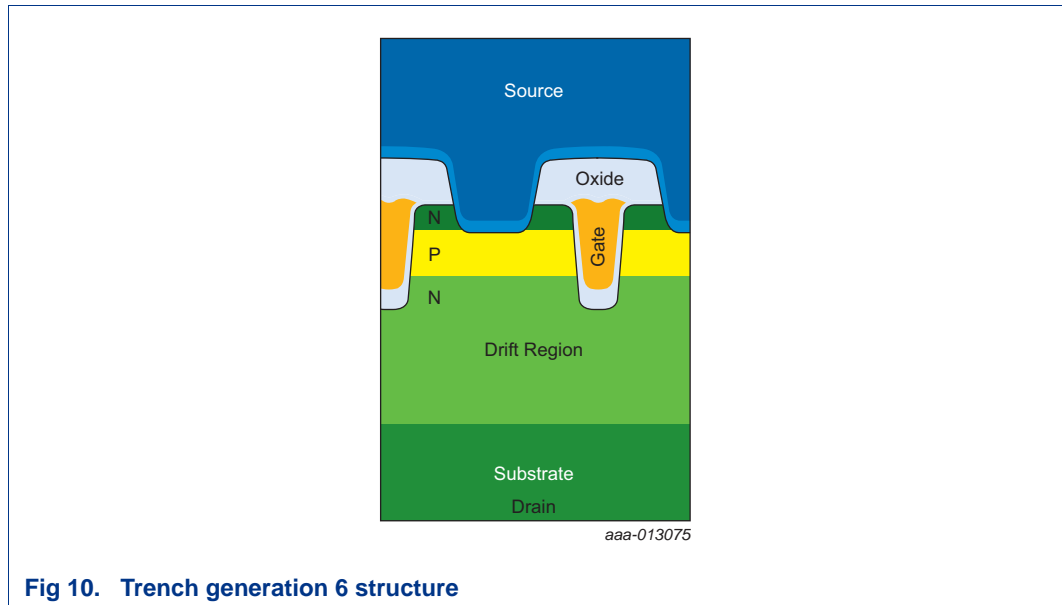
Fig 10. Trench generation 6 structure

7.9 **Q: In a half-bridge configuration one MOSFET is driven off, and the second MOSFET begins to turn on. The first MOSFET that should be off is turning back on again causing cross conduction and an overcurrent peak. What could be the cause? See Figure 11 for phenomena.**

Fig 11. **Blue V$_{GS}$ trace shows gate bounce and the red current waveform spiking when gate bounce occurs**
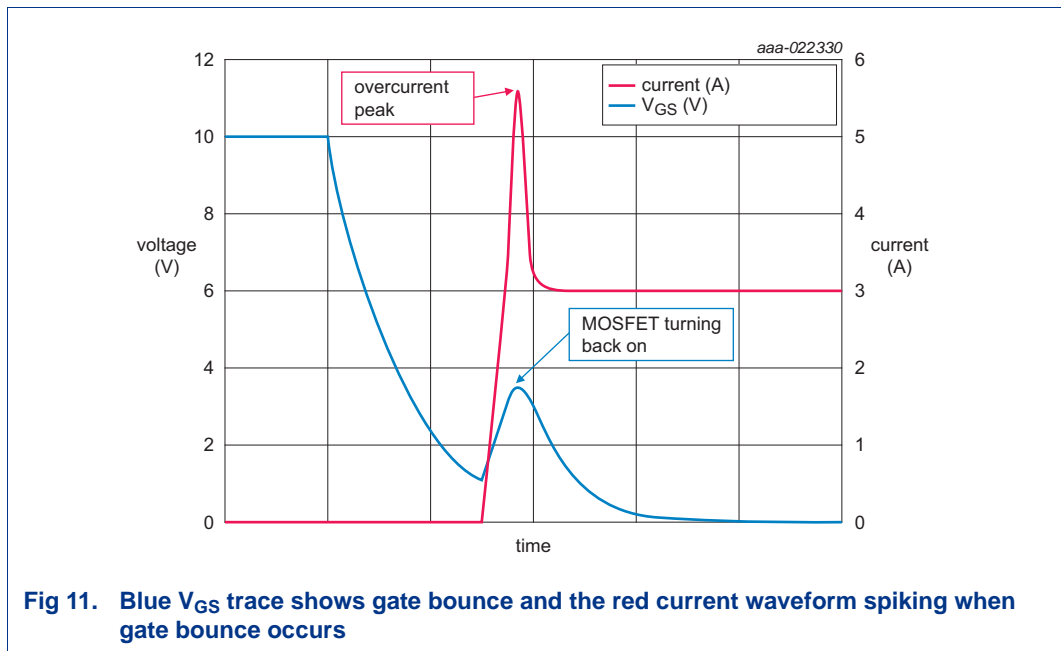
A: It is sometimes referred to as gate bounce. MOSFETs have internal stray capacitances coupling all three terminals and the gate is floating. The capacitors are inherent to the internal structure of a MOSFET, see Figure 12.

Fig 12. **MOSFET Schematic representing the internal capacitances**
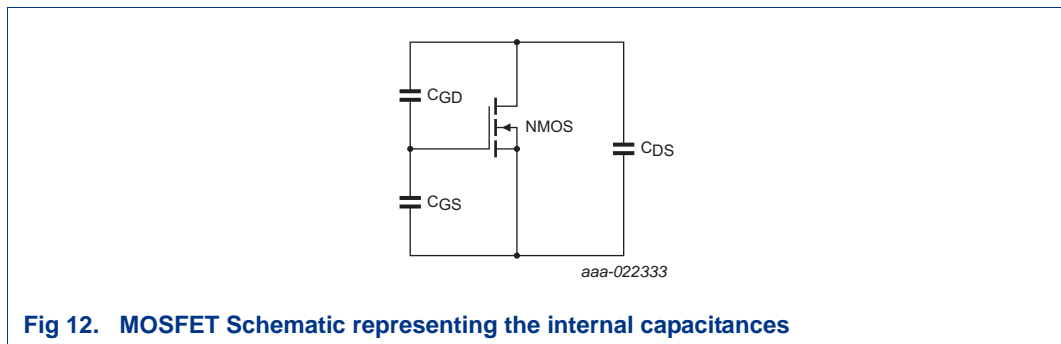
C_{GD} and C_{GS} form a capacitive potential divider. When a voltage appears across the drain and source of the MOSFET, it couples to the gate and causes the internal gate source capacitor to charge. If the voltage on the gate increases beyond the MOSFETs threshold voltage, it starts to turn back on which can cause cross conduction. The ratio of the capacitances C_{GD} and C_{GS} determines the severity of this effect.

Additional information

Figure 13 shows a simplified circuit that can exhibit this behavior. It could be a synchronous buck regulator or one leg of a 3-phase inverter. In both cases, the load is inductive. A current source represents the inductive element in this circuit.
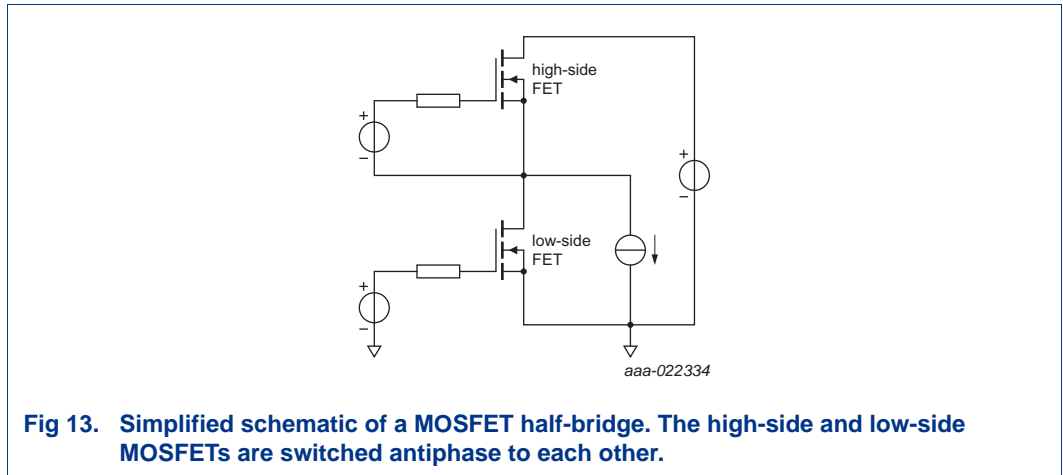
Fig 13. **Simplified schematic of a MOSFET half-bridge. The high-side and low-side MOSFETs are switched antiphase to each other.**
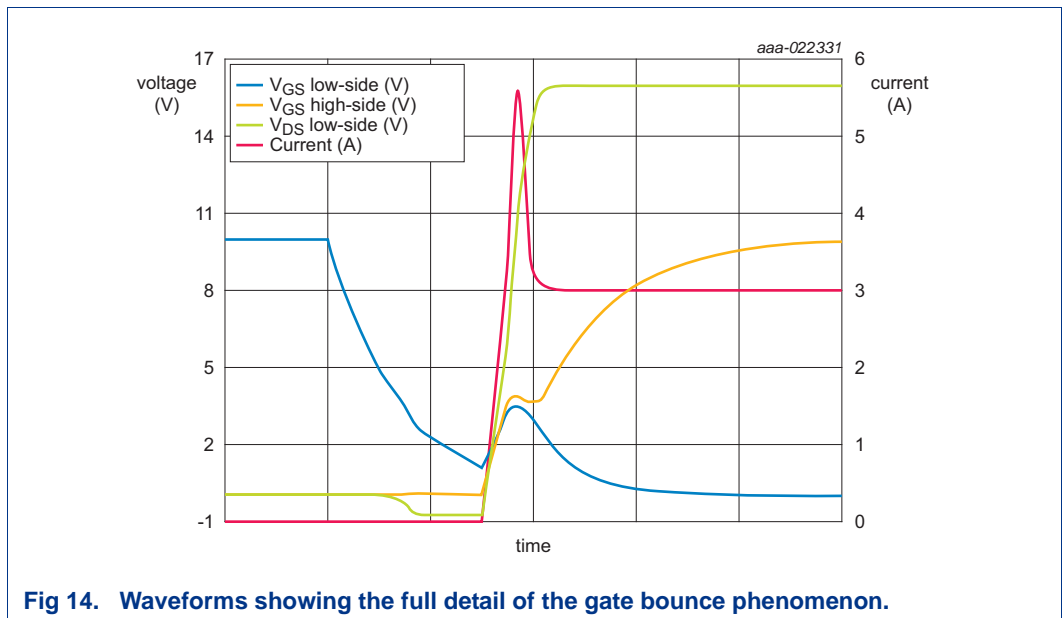
Fig 14. **Waveforms showing the full detail of the gate bounce phenomenon.**

The waveforms in Figure 14 show the critical part of the applications operation when the current commutates from one MOSFET to the other. In this instance, the high-side MOSFET is being switched on as the low-side one switches off. Current flows from the switch node. Note the low-side MOSFET behaves as a diode when it is switched off. This behavior is similar when current flows into the switch node. In this case, the high-side device becomes the synchronous rectifier. Referencing the waveforms in Figure 14, the blue low-side V_{GS} trace begins to drop and the low-side MOSFET turns off. The green low-side V_{DS} trace going negative indicates that it has switched off. The low side MOSFET body diode begins to conduct the inductive current and there is a V_F drop of approximately 0.7 V. The high-side MOSFET begins to turn on to a point where it conducts all of the load current. The low side diode turns off and the low-side V_{DS} can now increase to the supply voltage. However, as the V_{DS} rises, the dV/dt is coupled back to the low side gate through C_{GD}. The blue low-side V_{GS} trace begins to increase again. In this example, the gate voltage rises sufficiently above the threshold

voltage so that it is now turned back on again. Both high-side and low-side MOSFETs are on simultaneously. The current rapidly increases due to the short circuit across the supply as indicated by the red current trace.

There are several factors that influence this behavior, the most dominant of which is the gate resistor. If the gate resistor is set to a level where the gate driver cannot sink the capacitively coupled current, it must feed into the C_{GS}. It causes the gate source voltage to rise as can be seen in Figure 15.

Each waveform has a different external gate resistor. Increasing the gate resistor has a detrimental effect on the severity of the gate bounce.

Fig 15.   Effect of R_G on V_{GS}, and shoot-through current.
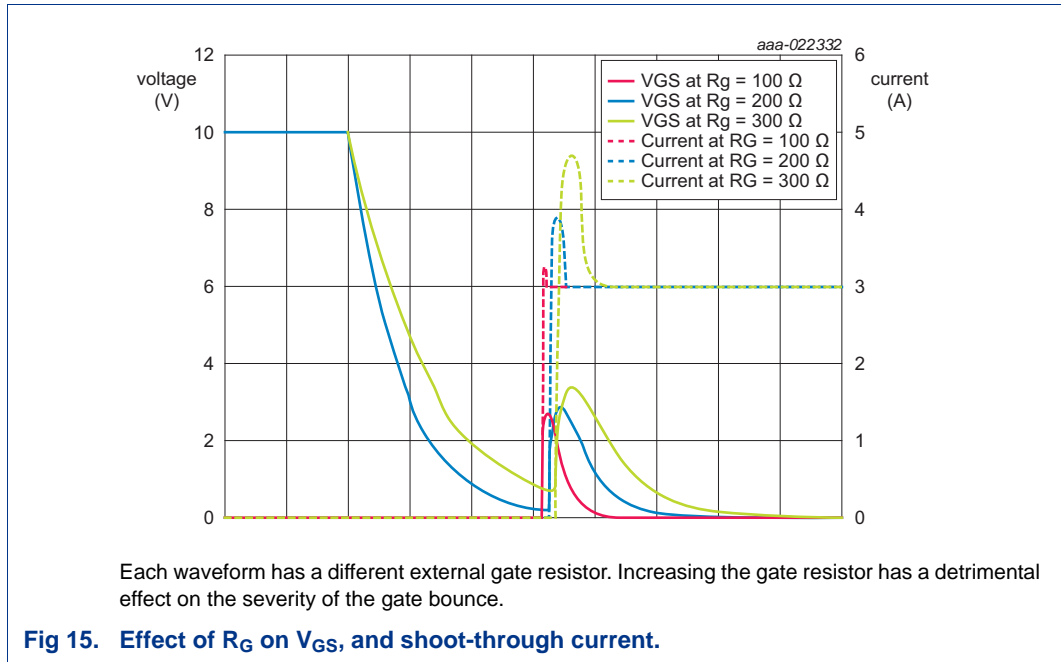
It is good practice to keep the external gate resistor as low as possible. In reality, there is a limit to how low this value can be, due to EMC considerations. Good design practices can be employed to improve EMC while maintaining a low enough value of gate resistor to prevent gate bounce. Simple alternatives to increasing the gate resistor include adding extra capacitors external to the MOSFET between gate and source, located close to the MOSFET connections. It helps with radiated emissions without affecting the gate turn off waveforms as much.

Other key factors include the MOSFETs threshold voltage (V_{th}). The lower V_{th} is, the more enhanced a MOSFET is for a given gate bounce voltage. It therefore increases the severity of the cross conduction. V_{th} is also temperature dependent. It reduces as die temperature increases, further compounding the severity.

7.10 Q: Does the BUK9Y29-40E fulfill the following requirements?

Table 1.   Turn on/off delay, rise time and fall time requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)} + t_r$	turn on delay time + rise time combined	$T_{amb} = 25\ ^\circ C$; $V_{DS} = 30$ V; $V_{GS} = 5$ V; $R_L = 50\ \Omega$; $R_{G(ext)} = 5\ \Omega$	8	13	18	ns
$t_{d(off)} + t_f$	turn off delay time + fall time combined	$T_{amb} = 25\ ^\circ C$; $V_{DS} = 30$ V; $V_{GS} = 5$ V; $R_L = 50\ \Omega$; $R_{G(ext)} = 5\ \Omega$	9	14	19	ns

A: Typical values of $t_{d(on)}$, t_r, $t_{d(off)}$, and t_f are given in the BUK9Y29-40E data sheet:

Table 2.   Turn on/off delays, rise time and fall time BUK9Y29-40E specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn on delay time	$T_{amb} = 25\ ^\circ C$; $V_{DS} = 30$ V; $V_{GS} = 5$ V; $R_L = 5\ \Omega$; $R_{G(ext)} = 5\ \Omega$	-	6	-	ns
t_r	rise time	$T_{amb} = 25\ ^\circ C$; $V_{DS} = 30$ V; $V_{GS} = 5$ V; $R_L = 5\ \Omega$; $R_{G(ext)} = 5\ \Omega$	-	7	-	ns
$t_{d(off)}$	turn off delay time	$T_{amb} = 25\ ^\circ C$; $V_{DS} = 30$ V; $V_{GS} = 5$ V; $R_L = 5\ \Omega$; $R_{G(ext)} = 5\ \Omega$	-	9	-	ns
t_f	fall time	$T_{amb} = 25\ ^\circ C$; $V_{DS} = 30$ V; $V_{GS} = 5$ V; $R_L = 5\ \Omega$; $R_{G(ext)} = 5\ \Omega$	-	5	-	ns

$t_{d(on)} + t_r$ must be between 8 ns and 18 ns. For the BUK9Y29-40E, this value is typically 13 ns.

$t_{d(off)} + t_f$ must be between 9 ns and 19 ns. For the BUK7Y29-40E, this value is typically 14 ns.

Minimum and maximum values for $t_{d(on)}$, t_r, $t_{d(off)}$, and t_f are not stated in NXP MOSFET data sheets. It is because accurate and repeatable measurements of these parameters, particularly t_r and t_f, very much depend on the test environment.

Even measurement probe positioning is critical because stray inductances, capacitances and coupling fields change when the probe is moved (unavoidable).

A good worst case estimate tolerance on these parameters is ±50 %, however these parameters have only a very small effect on MOSFET dynamic operation.

The typical BUK9Y29-40E fulfills these requirements, but if these parameters are slightly different, the consequences to the circuit switching performance are not significant. In the parametric test, a 50 Ω load resistor and 5 Ω external gate resistor are used. It is very unlikely that these values are the same as the values used in the application.

Gate drive characteristics, MOSFET capacitances and the nature of the load circuit have much more profound effects on the dynamic switching behavior of the MOSFET. Specifically, its power loss, efficiency and EMC performance.

8. Package and mounting

8.1 Q: On the drawing for the power SO8/LFPAK56 common footprint, there are no vias on the exposed pad. Are the addition of vias advised and, if so, which diameter?

A: If improved thermal resistance is required, vias can be added to the footprint. The effect of adding vias is discussed in *Section 3.5 of AN10874*.

Additional information

NXP has used 0.8 mm successfully but it does not mean that other sizes would not work.

The vias should be pre-filled with solder and hot air leveled, to give a flat surface, before the devices are placed.

If the vias are not pre-filled, there is a chance that the solder under the part is drawn into the vias, which may result in voids.

The extra process steps on the PCB and the potential problems mean that vias should not be used unless they are needed. Consult the manufacturing process engineers regarding surface mount and soldering process issues.

8.2 Q: How are devices tested for HV isolation tests? An application is tested at approximately 1 kV for HV isolation testing across various terminals and a significant value is seen across the MOSFET. Are there tests that perform HV isolation analysis and, if so, what are they?

A: We do not perform any HV isolation tests on any automotive MOSFETs or specify any HV isolation parameter in our data sheets. Insulation testing is only applicable to TO-220F packages (NXP SOT186A)

Additional information

HV isolation is specified for MOSFETs with insulated drain tabs or in modules with isolated bases. The test voltage applied in the NXP factory is 2.45 kV for 0.4 seconds (V_{rms} at 50 Hz).

8.3 Q: The efficiency of my DC-to-DC converter exceeds my requirements. Can I use smaller, higher RDS MOSFETs to save money?

Environmental conditions: 4-layer FR4 board at 105 °C ambient temperature.

A: Although it is possible to reduce efficiency, other factors become the constraints.

Additional information

The dominating factor is likely to be the temperature allowed at the solder joint between the MOSFET and the PCB. It is unlikely that 125 °C may be exceeded with FR4. If the dissipation is 2 W, the thermal resistance of the path from the MOSFET mounting base to ambient must be <10 K/W.

(125 °C − 105 °C)/2 W = 10 K/W

Some special arrangements are required to achieve this figure. However the customer has indicated an allowed dissipation of 2 W so they may have some more information about their system indicating that it is achievable.

If dissipation is increased to 5 W, the temperature at the mounting base reaches 155 °C which is probably not allowed. The alternative would be to improve the thermal resistance to <4 K/W, which is extremely challenging.

An indication as to what can be achieved, is given in *AN10874* and *AN11113*

The junction temperature of the MOSFET has not yet been mentioned. It is because it is only a few degrees higher than the mounting base. For example, consider an application for an LFPAK56 device, such as BUK7Y7R6-40E. The thermal resistance is 1.58 K/W. So for 2 W, the T_j would be 128.2 °C. For 5 W, it would be 133 °C (assuming T_{mb} can be held to 125 °C). Both of these values are well below the $T_{j(max)}$ of the MOSFET which is 175 °C.

So in summary, the limiting factor of what can be done with dissipation is the PCB and its thermal path to ambient, not the MOSFETs.

8.4 Q: What is the position of NXP on using Pb free solder for internal soldering (die attach, clip attach)?

A: NXP is a member of the DA5 working group. It is a project consortium comprising NXP, Bosch, Infineon, and ST. The goal is to find new solder materials or alternative die attach methods which do not use lead. The European directive 2011/65/Eu exemption (RoHS), allows the use of lead in high melting point solders until 2016. So far, no reliable and cost effective alternative process has been developed, especially where the requirements of AEC-Q101 are considered. An extension to the expiry date of this exemption was applied for in January 2015 by representatives of the electronics industry, including the DA5 working group.

The End of Life Vehicle (ELV) Directive (2000/53/EG) also applies. A similar extension to the Pb free exemption was applied for by the DA5 group in November 2013. It is expected that if approved, this directive allows the use of Pb based solders until 2018 at the earliest. It has been requested that the EU aligns the Pb free exemption between the ELV directive and the RoHS directive.

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9. SPICE models

9.1 Q: Is there is a large difference between the data sheet and the SPICE model behavior and in particular, the gate charge characteristics?

A: There is a strong similarity between the data sheet characteristics and the NXP SPICE models at 25 °C. It is especially true for transfer curve, $R_{DS(on)}$, diode characteristic, and gate charge. The SPICE model also accounts for the package parasitic resistances and inductances.

Additional information

In PWM circuits, the SPICE model gives quite a good similarity to the behavior of the real device. The SPICE model can therefore be used to give a good indication of the switching losses at turn-on and turn-off, as well as the conduction losses.

The SPICE model is only correct at 25 °C, the $R_{DS(on)}$ versus temperature characteristic can be used to estimate conduction losses at higher temperatures. Switching losses are known not to change significantly with temperature.

The SPICE model also reflects a typical device according to the data sheet characteristics.

The method of creating models has been continuously improved over time. The latest model creation process used for Trench generation 6 devices and newer technologies results in models which closely match measured device behavior.

9.2 Q: Why does the spice model not match the data sheet?

A: The SPICE models provided by NXP are generated from measurements performed on a sample of devices. Several parameters such as transfer characteristics, output characteristics and gate charge are used. Values for parasitic package impedances and the data sheet maximum $R_{DS(on)}$ value are combined to produce a model that emulates the behavior of the sample MOSFETs.

Additional information

It is important to note that the spice models generated by NXP:

– represent typical parts that can be found within the production distribution.

– are set close to the maximum R_{DSon} of the part without adversely affecting the other model parameters.

– are only valid for $T_j = 25$ °C.

Customers wishing to do design validation using a spice model, are advised to proceed with caution given the information provided above. NXP encourages designers to perform Monte Carlo simulations and use tolerance stacks in their simulation design. These factors permit part to part variation of their whole system to be accounted for.

NXP can advise on what reasonable levels of tolerance on key parameters for the MOSFET would be.

10. MOSFET silicon technology

10.1 Q: What is drift engineering?

A: Drift engineering is optimizing of the drift region between the bottom of the trench and the epi/substrate interface (light green area). The drift region supports most of the drain-source voltage in the off state. The purpose of drift engineering is to reduce the resistance of the drift region while maintaining the drain-source breakdown voltage $V_{(BR)DSS}$ capability (see Figure 16).
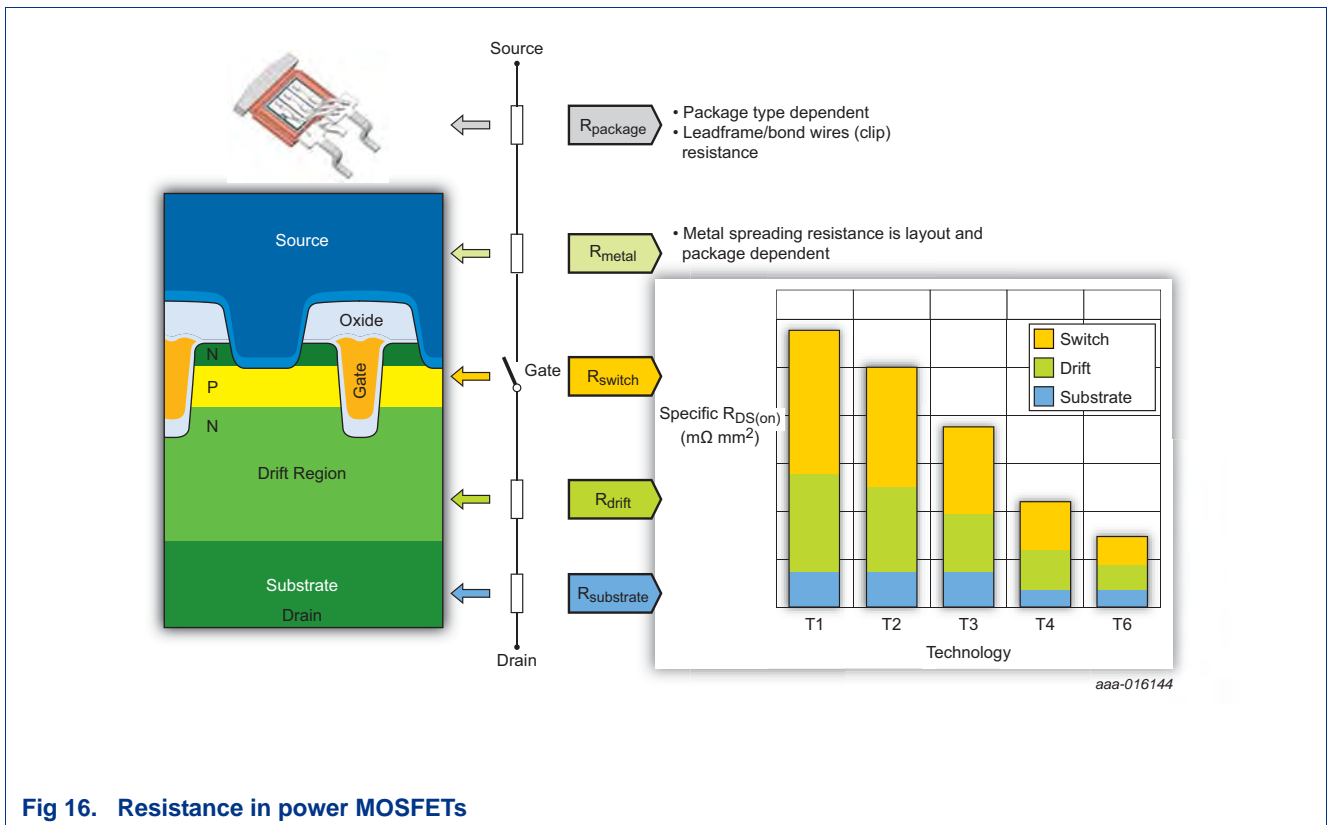
Fig 16. Resistance in power MOSFETs

10.2 Q: What is obtained from reduced cell pitch?

A: Reduced cell pitch generally results in lower resistance and higher capacitance. The goal of each new generation of MOSFET technology is to reduce $R_{DS(on)}$ without a large increase in capacitance that usually accompanies reduced cell pitch. Reduced cell pitch also reduces SOA capability (linear mode operation) but improves avalanche capability.

10.3 Q: What is obtained from a shorter channel?

A: Shorter channel gives a lower $R_{DS(on)}$ and a lower C_{GS} capacitance simultaneously. It has higher leakage current and the transfer curve (I_D versus V_{GS} characteristic) becomes more dependent on V_{DS}. It is also observed in the output characteristics.

10.4 Q: What is obtained from thick bottom oxide?

A: Thick bottom oxide refers to gate oxide at the bottom of the trench (see Figure 16). It is made thicker than the gate oxide at the side of the trench. It acts as a thicker dielectric between the gate and the drain resulting in a much lower C_{GD} value.

11. Supply and availability

11.1 Q: What statements can be made concerning the long-term availability of previous generations of TrenchMOS parts?

A: NXP continues to supply older products where the volumes of manufacture are economically viable. The sales price margin is commercially viable and there are no manufacturing reasons which prevent manufacture.

A Discontinuation of Delivery (DoD) document notifies key customers (including distributors), when a part is planned to be withdrawn. It allows customers to make arrangements to buy sufficient products for future requirements and if necessary qualify alternative products.

12. EMC

12.1 Q: If EMC issues are encountered when substituting Trench generation 6 parts for competitor parts, what advice is available? Can the application note *AN11160 Designing RC snubbers* help?

A: In this case, optimizing the RC snubber for the NXP MOSFET is necessary.

Additional information

EMC performance depends on many factors, some of which depend on layout parasitics, circuit components and the power MOSFET. For applications such as half bridges, 3-phase inverters, DC-to-DC converters etc., a snubber is often needed. It helps to reduce oscillations across the MOSFET drain and source terminals to acceptable levels. These oscillations would travel along conductors which can act as antennae. However, the snubber for the incumbent part is likely to be different from what is needed for the NXP device. It is because the MOSFETs are made from different technologies with different dynamic characteristics.

We would recommend following the process described in *AN11160* that was written specifically for these situations.

13. Leakage, breakdown and MOSFET characteristics

13.1 Q: How does drain current (I_{DSS}) vary with respect to temperature?

A: The fundamental relationship between drain leakage current and temperature is exponential in form. The data sheet gives maximum values of I_{DSS} at T_j = 25 °C and 175 °C. This example is specific to NXP Trench generation 2 technology but the same principles can be applied for other NXP technology. An exponential fit to these points provides the plot of Figure 17. It is also in line with some testing which is performed during the development of new MOSFET technologies.

Additional information

Figure 18 is the same curve, plotted with a log scale for I_{DSS} to ease reading the value of 20 µA at 50 °C. These values are for a V_{DS} at the rated voltage. Reducing voltage reduces leakage current.
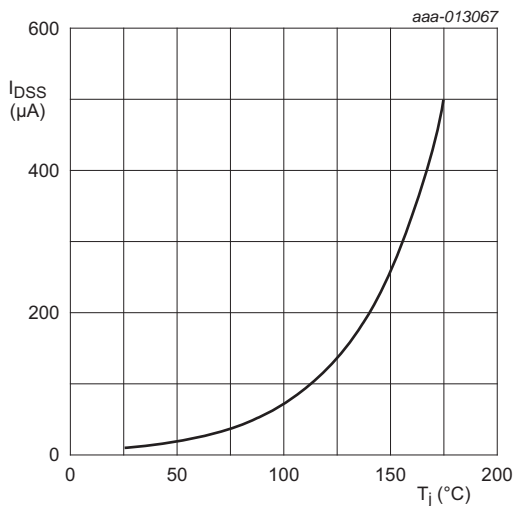
I_{DSS} = 10 µA (25 °C), I_{DSS} = 500 µA (175 °C),

Fig 17. **I_{DSS} as a function of temperature, linear axes**
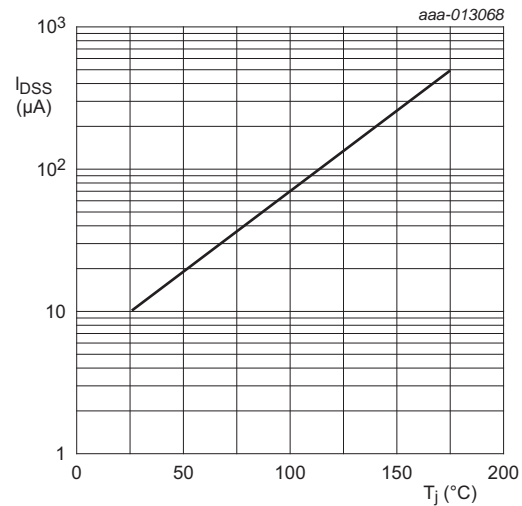
I_{DSS} = 10 µA (25 °C), I_{DSS} = 500 µA (175 °C),

Fig 18. **I_{DSS} as a function of temperature, log - linear axes**

13.2 Q: What is the relationship between breakdown voltage $V_{(BR)DSS}$ at I_D = 250 µA) and drain leakage current (I_{DSS})? Both state the same V_{DSS} value but the drain current is different.

A: Although these two parameters reference the voltage rating of the part, they look at different characteristics of the product. Drain leakage current (I_{DSS}) looks at the characteristic for V_{DS} at the rated voltage. The test applies a voltage, and checks that the current is below the limit.

Additional information

The breakdown voltage of a device $V_{(BR)DSS}$ is the V_{DS} required to cause a drain current of 250 µA to flow. It is slightly higher than the rated voltage of the device and the actual voltage varies for the same nominal type due to manufacturing

variations. The minimum stated in the data sheet is the rated voltage. Breakdown voltage looks at the characteristic of the part when it is in avalanche. The mechanisms causing leakage current and avalanche current are different.

13.3 Q: Is the standard level gate device BUK7Y28-75B guaranteed to work with a 7 V gate drive at −40 °C for 25 A?

A: NXP has a high degree of confidence that this scenario would be OK even in the worst case. However, it cannot be 100 % guaranteed by a production test at 25 °C.

Additional information

Referring to Figure 19, the typical gate threshold voltage $V_{GS(th)}$ is 3 V. It rises to approximately 3.5 V at −55 °C (i.e. a rise of approximately 0.5 V). The highest $V_{GS(th)}$ rises from approximately 4 V to 4.5 V (again, approximately 0.5 V). So in the worst case at −55 °C, the threshold voltage shifts by 1.5 V from the typical 25 °C value.

Looking at Figure 20, it would shift the gate drive curve from 7.0 V to 5.5 V for a worst case device (1.5 V shift).
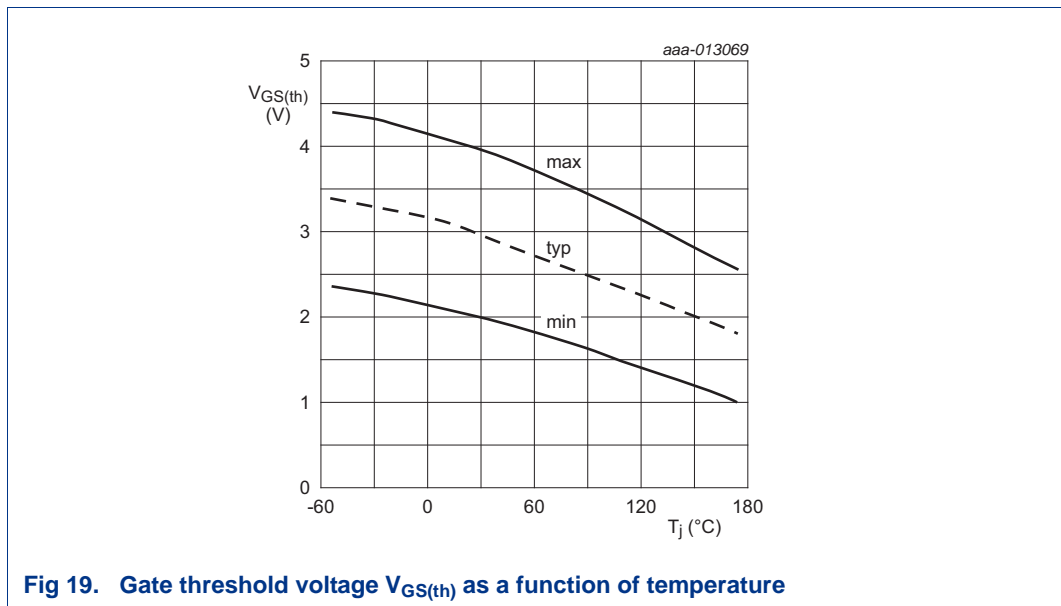
Fig 19. Gate threshold voltage $V_{GS(th)}$ as a function of temperature
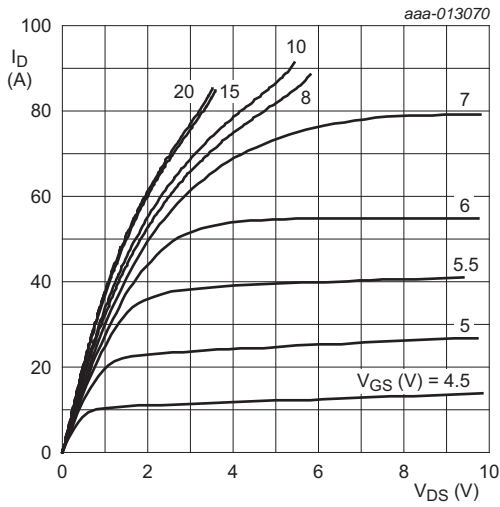
| **Fig 20.** | Drain current as a function of drain-source voltage: typical values | **Fig 21.** | Drain-source on-state resistance as a function of drain current: typical values |
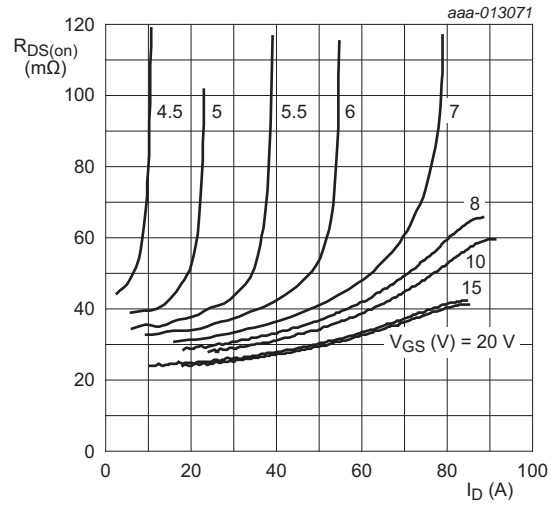
The 5.5 V drive curve allows more than 25 A and is still in the linear $R_{DS(on)}$ region of the output characteristic.

The $R_{DS(on)}$ values for the 5.5 V characteristic at 25 A in Figure 21 is pessimistic for operation at −40 °C. It uses the 25 °C $R_{DS(on)}$ curves, and the mobility increases with lower temperatures making the $R_{DS(on)}$ better. The threshold voltage increase has already been accounted for.

It explains why a 7 V gate drive at −40 °C would be OK for this particular standard level gate device (BUK7Y28-75B). The same principles can be applied to other NXP devices. However, the customer must judge whether there is adequate margin in the design, as the result may be slightly different from what is observed.

13.4 Q: What is the lowest voltage $V_{(BR)DSS}$ to be expected at −40 °C for a 40 V device using Trench generation 6?

A: The following principle could be applied to any NXP MOSFET technology at any breakdown voltage rating. In the data sheet, the values for minimum drain-source breakdown voltages are specified at −55 °C and 25 °C. The correlation between $V_{(BR)DSS}$ and temperature is approximately linear over this range. Therefore, a straight line can be plotted at Temperature (−55 °C and 25 °C) versus $V_{(BR)DSS}$ (at −55 °C and 25 °C).

For example: a 40 V Trench generation 6 part, has a $V_{(BR)DSS}$ at −55 °C of 36 V and 40 V at 25 °C. Using linear interpolation, gives a $V_{(BR)DSS}$

of 36.75 V at −40 °C.

13.5 Q: What factors affect the value of drain current according to the transfer characteristic graph for BUK9275-55A, especially over the V_{GS} range of 2.2 V to 3.0 V?

A: The answer to this question is not simple - there are several factors which would affect the I_D value.

1. The graph depicted in Figure 22 is typical. The BUK9275-55A MOSFET has a distribution of parameter values within the production tolerance limits. The graph is only intended to illustrate how I_D, V_{DS} and V_{GS} are related when the MOSFET is operating for a particular V_{DS} condition. $V_{GS(th)}$ has a significant influence on the characteristic of a particular device. Temperature is also a major factor. The limiting values and characteristics listed in the data sheet should be used for circuit design.

2. Junction temperature T_j strongly affects the I_D / V_{GS} characteristic. The graph in Figure 22 is for T_j = 25 °C and T_j = 175 °C. The same graph for the same part with T_j = −55 °C, would be very different. The mode of operation preferred by the customer is with V_{GS} in the range 2.2 V to 3 V in the saturation region before full enhancement. In this mode, the MOSFET power dissipation is likely to be significant. As a result, the junction temperature may be high. Figure 22 demonstrates how I_D changes with T_j for a given V_{GS} value.

3. A dashed vertical red line on the graph is shown at V_{GS} = 2.2 V. If T_j increases from 25 °C to 175 °C, I_D approximately doubles (from approximately 1 A to 2 A). However, at V_{GS} = 2.8 V (dashed vertical green line), the same junction temperature change has no effect on I_D. At V_{GS} > 2.8 V, an increase in T_j results in a decrease in I_D.
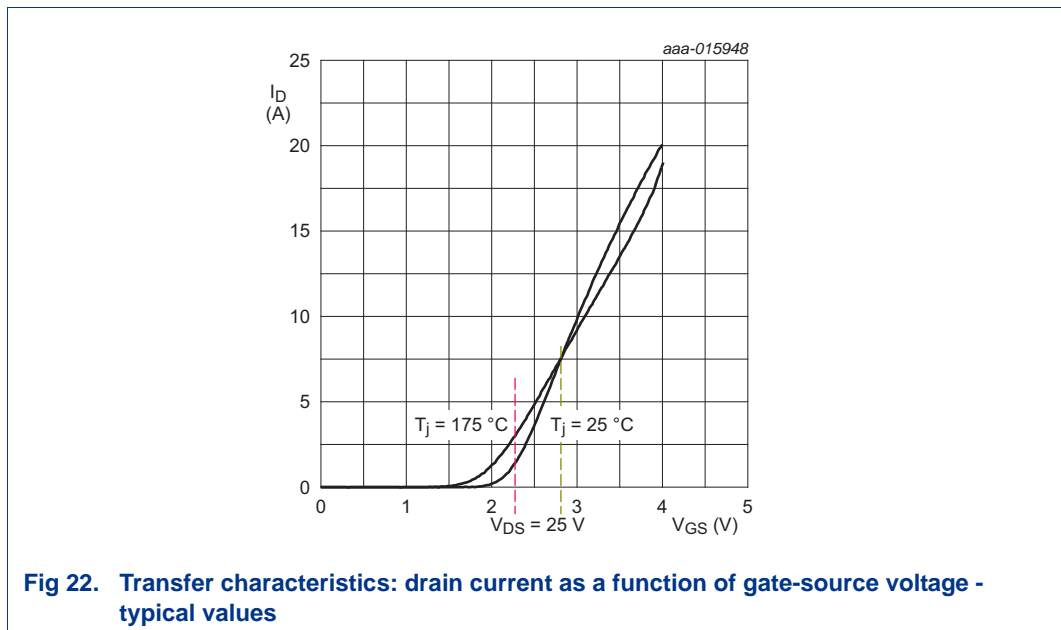
Fig 22. Transfer characteristics: drain current as a function of gate-source voltage - typical values

It is clear that the relationship between the MOSFET parameters is complex and their relationship with the thermal environment is also complex.

13.6 Q: Can NXP provide C_{GD}, C_{GS} and C_{DS} numerical values for $T_j = -55$ °C and $T_j = +175$ °C (at $V_{GS} = 0$ V, $V_{DS} = 16$ V)? If it is impossible to test, a theoretical one is also acceptable. A graph is provided in Figure 23, but it is for $T_j = +25$ °C.

A: Unfortunately NXP cannot supply values for these capacitances at the extremes of the MOSFET operating temperature range requested. It is due to the limitations of our parametric test equipment. However, we can comment on how these capacitances vary with temperature and the MOSFET terminal voltages.

Additional information

C_{iss} is the input capacitance formed by the parallel combination of C_{GS} and C_{GD}, and C_{GS} dominates. C_{GS} is formed across the gate oxide so it does not vary significantly with temperature or the MOSFET terminal voltages. As C_{GS} depends on gate oxide thickness and other defined die feature dimensions, it should not vary much between samples.

C_{rss} is the reverse transfer capacitance which is essentially the gate-drain capacitance (C_{GD}). It is formed across the MOSFET body diode depletion layer. This layer becomes thicker, as the reverse voltage (V_{DS}) across it increases. C_{rss} increases as V_{DS} decreases. C_{rss} has a greater variability than C_{iss} because it depends on the body diode depletion layer.

C_{oss} is the output capacitance formed by the parallel combination of C_{DS} and C_{GD}. The drain-source capacitance (C_{DS}) also dominates this capacitance. It varies with V_{DS} in a similar way to C_{rss} varying with V_{DS} and it has similar variability to C_{rss} for the same reasons.

These relationships are illustrated on the data sheet graph depicted by Figure 23. It has been observed that switching losses only slightly increase at $T_{j(max)}$, in the order of 10 %, since the capacitances only marginally change. Other factors can influence switching behavior, especially where the gate driver current capability changes significantly with temperature. The depletion layer thickness varies in proportion to the square root of the absolute temperature in K and it affects C_{rss} and C_{oss}.
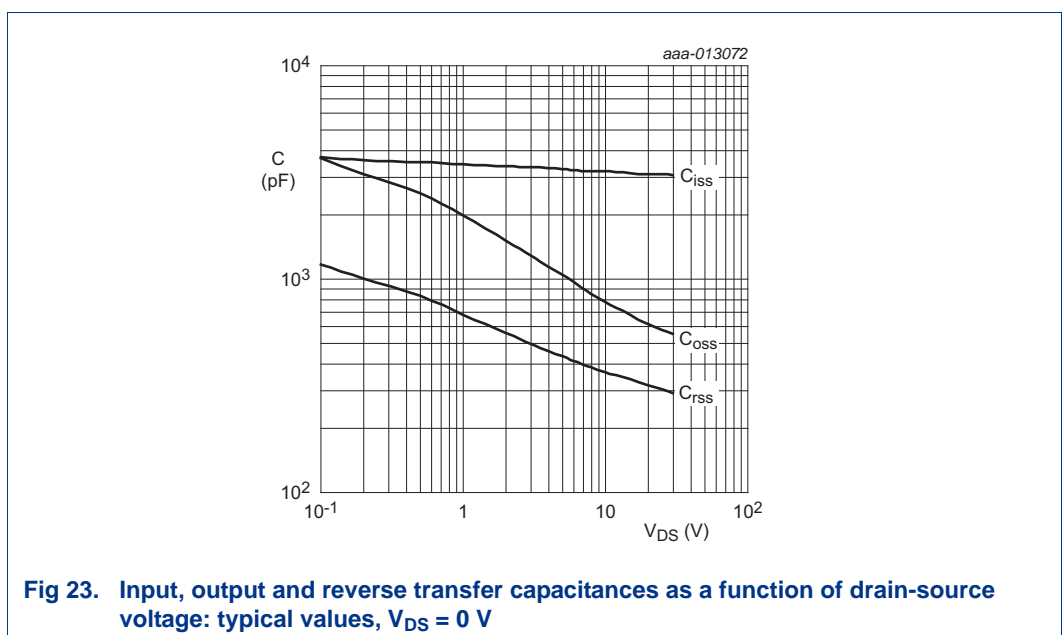
Fig 23. Input, output and reverse transfer capacitances as a function of drain-source voltage: typical values, $V_{DS} = 0$ V

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13.7 Q: Can NXP provide the minimum V_GS threshold values for T_j from −55 °C to +175 °C? A graph is already in the data sheet. However, the numerical data of minimum values in the range of −55 °C to +175 °C are required for a standard level gate threshold.

A: Worst case values of minimum and maximum $V_{GS(th)}$ should be used for design purposes. They are given in the data sheet Characteristics (see Table 3).

Additional information

Table 3.   Limiting values
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C	2.4	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = −55 °C	-	-	4.5	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C	1	-	-	V

These values are guaranteed worst case values. In this case, the 175 °C minimum $V_{GS(th)}$ is not less than 1 V. The −55 °C $V_{GS(th)}$ is not greater than 4.5 V.

13.8 Q: Can NXP provide the inherent R_G component value with T_j from −55 °C to +175 °C?

A: The measured R_G value is in the range of 1 Ω to 3 Ω and it does not vary significantly with temperature. In our general MOSFET characterization, it is presently not possible to test R_G over the temperature range.

Additional information

In a circuit such as the 3-phase motor drive circuit, switching speed is not usually critically important. The PWM frequency is usually moderate (<50 kHz). However, to mitigate emissions due to high dV/dt, the circuit designer often deliberately slows the switching of the MOSFET.

A low value (10 Ω) fixed resistor connected between the gate driver output and the MOSFET gate helps to stabilize the gate driver voltage and damp out any voltage transients or oscillations.

Often, even higher external gate driver resistor values are chosen to slow down the gate driver and reduce the EMI effects of the MOSFET switching.

13.9 Q: How is the maximum permissible drain current estimated, at the point of V_{DS} = 0.1 V, from the SOA curve of the BUK9K12-60E shown in [Figure 24](#)? Some manufacturers described down to the V_{DS} value in their SOA curves.
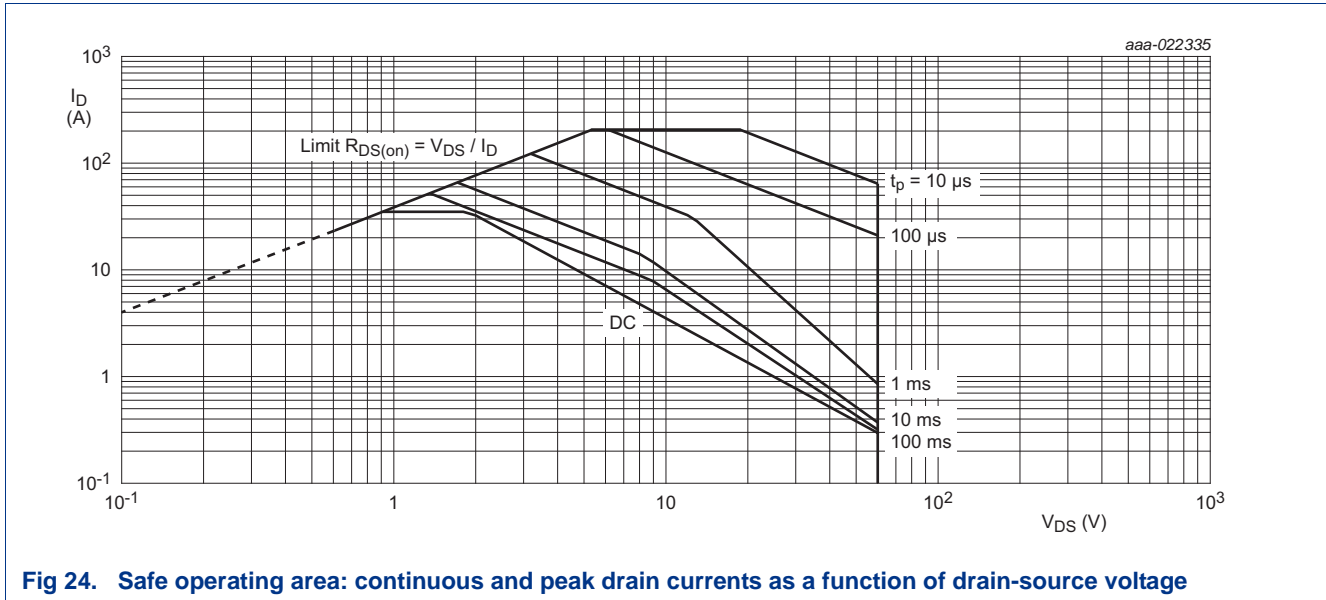
Fig 24. Safe operating area: continuous and peak drain currents as a function of drain-source voltage

A: The minimum current that is expected at a V_{DS} of 0.1 V can be calculated from the maximum (175 °C) $R_{DS(on)}$ value (26 mΩ):

Table 4. $R_{DS(on)}$ values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = 5 V; I_D = 15 A; T_j = 25 °C	-	9.5	11.5	mΩ
		V_{GS} = 5 V; I_D = 15 A; T_j = 175 °C	-	21.5	26	mΩ

Additional information

The drain current that flows with these conditions is 0.1/0.026 = 3.846 A. The maximum die temperature is the critical factor. Do not allow it to exceed 175 °C.

However, if the $R_{DS(on)}$ is not at the top limit of the value range or the die temperature is lower, it is lower. As a result, the corresponding drain current is proportionately higher.

The maximum $R_{DS(on)}$ is 11.5 mΩ at T_{mb} = 25 °C. The maximum die temperature is likely to be higher than 25 °C in most applications.

If the mounting base temperature is maintained at 100 °C or less, the (fully ON) MOSFET can safely carry a continuous current up to 35 A.

Table 5. I_D values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 5 V	-	-	35	A
		T_{mb} = 100 °C; V_{GS} = 5 V	-	-	35	A

The (fully ON) MOSFET can also sustain a current pulse of 204 A for a period up to 10 μs.

Table 6. **I_{DM} values**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DM}	peak drain current	T_{mb} = 25 °C; $t_p \le$ 10 μs	-	-	204	A

13.10 Q: Is the BUK7K52-60E drain current specified individually for each (FET1 and FET2) or as a total of 15.4 A?

Table 7. **Drain specifications**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge$ 25 °C; $T_j \le$ 175 °C	-	-	60	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C	-	-	15.4	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	-	-	32	W

A: The ratings given on the data sheet are for each individual MOSFET in the device.

Additional information

Although there are two MOSFETs housed within the package, they are fully electrically isolated from each other.

However, as the MOSFETs share a common package, there is a small amount of thermal coupling between the two MOSFET dies through the plastic package material. The heat generated by the power dissipated in one MOSFET increases the temperature of the other, even though the other may not be dissipating power. In an application, there is also an external thermal coupling path via the PCB to which the device is mounted. In practice, it is the main thermal coupling mechanism between the two dies.

To guarantee long-term reliability, it is very important that the junction temperature of either of the dies is never allowed to exceed 175 °C.

The individual MOSFET mounting bases are the main exit routes for heat generated in the dies. In practice, the mounting bases are soldered to copper pads on a Printed-Circuit Board (PCB). They provide the electrical connections to the MOSFET drains and heat sinking. Both MOSFETs in the package should operate at their rated power/current when their mounting bases are maintained at 25 °C. However, it is very difficult to achieve in practice and de-rating must be done in most cases.

Example:

Using a BUK7K52-60E for two MOSFETs in a half-bridge, driving an inductive load.

Assumptions:

MOSFETs conduct alternately, never together.

Switching losses are neglected.

PCB material is standard FR4.

Standard FR4 PCB material has a maximum operating temperature of 125 °C, although special higher temperature materials are available.

The maximum temperature of the MOSFET mounting bases is limited to 125 °C by appropriate PCB cooling. The maximum de-rated power that can be dissipated in one MOSFET is 32/3 = 10.67 W.

The temperature rise of the die above the temperature of its mounting base is 10.67(W) * 4.68 (K/W) = 49.9 K.

Therefore, the maximum die temperature is 125 + 49.9 = 174.9 °C, which is marginally safe.

Worst case $R_{DS(on)}$ at T_j = 175 °C = 101 mΩ.

Maximum allowed current = $\sqrt{(P/R_{DS(on)})}$ = 10.28 A.

Note: This calculation is a theoretical example. The PCB cooling required to maintain a 125 °C mounting base temperature with 10.67 W power dissipation would be very difficult to achieve in practice.

14. MOSFET reliability

14.1 Q: How is the FIT-rate calculated?

A: FIT (Failure In Time) is commonly used to express component reliability. It is defined as the number of failures occurring in 1×10^9 hours (1 billion hours).

At any elapsed time (t), the reliability (R) of a group of operating semiconductors is:

$R(t) = (n_o - n_f)/n_o$

Where:

n_o is the original sample size and n_f is the number of failures after time t.

Over the standard time of 10^9 hours, it approximates to $F = (1/n_o)*(n_f/t)*10^9$.

<u>Accelerated testing</u>

A major factor in determining the reliability of a semiconductor is the total stress applied by the application. Operating temperature results from ambient temperature and the heat due to power dissipation. It is the most important applied operating stress where a product is otherwise generally operated within its ratings.

The Arrhenius equation is used to model the effect of temperature on component failure rate:

$$\text{Acceleration factor} = e^{(EA/k)*(1/T1 - 1/T2)} \qquad (7)$$

Where:

Ea = activation energy (eV)

k = Boltzmann constant (8.60×10^{-5} eV / K)

T1 = operating temperature (°C)

T2 = reliability test temperature (K referenced to absolute zero)

Accelerated testing makes components perform at high levels of (thermal) stress. The results are then extrapolated to convert short life under severe conditions into the expected life under normal conditions.

Under accelerated life test conditions:

$$F = (n_f/n_o*A*t) * 10^9 \text{ FITs} \qquad (8)$$

Time t is now equal to A*t, where A is the acceleration factor.

Based on the life-test results for an example part, the FIT data provided in <u>Table 8</u> has been calculated. Note that an adjustment is made to the number of failures based on Poissons probability distribution. It is used to indicate the number of failures expected in a larger sample depending on the confidence level. It is described in *JEDEC JEP122F Section 5.18.1.4* and in numerous other references.

Table 8.   Calculated FIT data

Test name	High Temperature Reverse Bias (HTRB) + High Temperature Gate Bias (HTGB) + High Temperature Storage Bias (HTSL)				
Test temperature	175	°C			
Number of device hours	35.051.000				
Number of observed failures	0				
Confidence level	90	%			
Activation energy	0.7	eV			
Failure rate					**Unit**
Failure rate at	125	°C	at 90 % confidence	6.725	FIT
Failure rate at	85	°C	at 90 % confidence	0.688	FIT
Failure rate at	55	°C	at 90 % confidence	0.086	FIT
Failure rate at	25	°C	at 90 % confidence	0.0007	FIT
MTBF					**Unit**
Mean time before failure at	125	°C	at 90 % confidence =	1.49×10^8	hour
Mean time before failure at	85	°C	at 90 % confidence =	1.45×10^9	hour
Mean time before failure at	55	°C	at 90 % confidence =	1.16×10^{10}	hour
Mean time before failure at	25	°C	at 90 % confidence =	1.40×10^{11}	hour

15. References

[1]   AN11158 — *Understanding power MOSFET data sheet parameters*

[2]   AN10273 — *Power MOSFET single-shot and repetitive avalanche ruggedness rating*

[3]   AN10874 — *LFPAK MOSFET thermal design guide*

[4]   AN11113 — *LFPAK MOSFET thermal design guide - Part 2*

[5]   AN11160 — *Designing RC snubbers*

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17. Tables

18. Figures

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